Characterization of Systematic and Random Diode Mismatches in Antiparallel-Diode Mixers

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***Abstract*—Diode mismatch in an antiparallel-diode (APD) mixer results in an unwanted virtual local-oscillator (LO) leakage. At a radio system level, the virtual LO leakage is primarily a challenge of meeting spurious emission requirements. At a device level, it is a challenge of circuit yield, determined by the statistical variation in diode mismatch of a semiconductor fabrication process. This paper introduces methods of characterizing diode mismatch in APD mixers. The parameters of these characterization methods can be used to make an informed selection of the fabrication process, diode size, and LO pump power for reduced virtual LO leakage and improved yield.**

***Index Terms*—Microwave mixers, millimeter-wave mixers.**

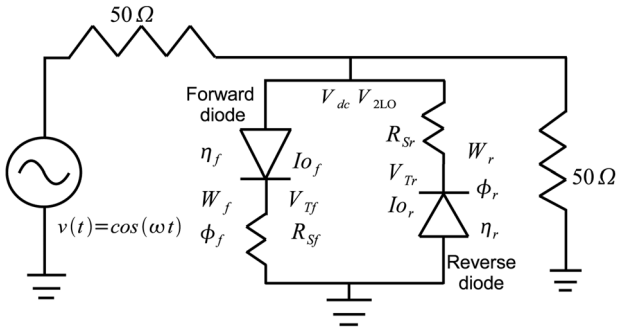

Fig. 1. Model of the APD circuit with diode mismatch.

I. Introduction

FREQUENCY conversion from an intermediate frequency to a radio frequency in a subharmonic mixer involves mixing the intermediate frequency with a multiple of the local-oscillator (LO) pump frequency. A subharmonic mixer switching at a virtual LO frequency, which is twice the pump frequency, can be built by connecting two diodes, as shown in Fig. 1. These are referred to as antiparallel-diode (APD) mixers. They are employed to overcome the output-power limitations of fundamental oscillators at millimeter-wave frequencies [1], [2].

An APD mixer with perfectly matched diodes generates no products at the even harmonics of the LO pump frequency. However, diode mismatch results in an unwanted virtual LO leakage at twice the LO pump frequency [2], [3].

The virtual LO leakage generated due to diode mismatch is reduced at the system level by the use of passive baluns or filters [4]. The use of baluns or filters increases the cost [5]. Moreover, in low intermediate frequency or direct conversion systems, the removal of virtual LO leakage through filters or baluns is not feasible. Such applications require the reduction of virtual LO leakage at the device level, without the use of passive filters or baluns.

Diode mismatch caused by variability in the fabrication process is beyond the control of APD mixer designers [6]. Process variability results in a statistical variation in diode mismatch and, consequently, a statistical variation in virtual LO leakage. This results in reduced yield of APD mixers fabricated using a monolithic-microwave integrated-circuit (MMIC) process.

The extent of statistical variation in diode mismatch caused by process variability is dependent on the fabrication process and diode size. Hence, the choices of the process and the diode size are important considerations in attempts to reduce virtual LO leakage and simultaneously improve yield in a semiconductor wafer. Characterization of diode mismatch will enable an intelligent selection of process and size. However, methods of characterizing diode mismatch do not exist yet. Furthermore, there is no known method of calculating optimum LO pump power that is specific for a given diode size that results in reduced virtual LO leakage and improved statistical yield in APD mixers.characterizing diode mismatch do not exist yet. Furthermore, there is no known method of calculating optimum LO pump power that is specific for a given diode size that results in reduced virtual LO leakage and improved statistical yield in APD mixers.

This paper introduces the theory and practice behind the methods of characterizing diode mismatch. It is also used to show that virtual LO leakage resulting from process variability can be reduced by the use of appropriate diode size and an optimum LO pump power. A method to calculate the optimum LO pump power for a given diode size is introduced. These methods provide a strategy to design APD mixers for reduced virtual LO leakage and improved statistical yield. These methods are useful in applications where low-intermediate-frequency operation and low component cost are critical.

This paper was motivated by the need to reduce the cost of gallium arsenide (GaAs) MMIC transmitters, which use an APD mixer for subharmonic mixing. The removal of virtual LO leakage through the use of a filter or a balun is expensive [4], [5]. An appropriate selection of diode size that reduces virtual LO leakage improves cost and circuit yield.

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Any degradation in mixer conversion gain resulting from the use of a diode size, selected purely on the basis of its virtual LO leakage performance, is easily offset in integrated transmitters by the use of amplification in the signal path, which is relatively cheaper than filtering [5].

II. Diode Mismatch

Diode mismatch results in different intrinsic diode parameters for the diodes marked forward and reverse (refer to Fig. 1). The resulting asymmetries in diode saturation currents, thermal voltages, and series resistances are represented by (I_{of}, I_{or}), (V_{Tf}, V_{Tr}), and (R_{sf}, R_{sr}) for forward and reverse diodes, respectively [3], [6]–[8]. The diode thermal voltages can be further represented as

$$V_{Tf} = \frac{\eta_f k T_f}{q} \quad V_{Tr} = \frac{\eta_r k T_r}{q} \tag{1}$$

where η_f and η_r are the ideality factors of forward and reverse diodes, respectively; T_f and T_r are the forward and reverse junction temperatures, respectively; k is a Boltzmann constant, and q is the electron charge [6].

Diode mismatch in an APD mixer is either due to random variability in the fabrication process or systematic effects arising from inherent layout asymmetry [6], [8]. Random process variability in an APD circuit population has been found to result in a correlation between the statistical variation in I_{of}/I_{or} and the statistical variation in V_{Tf}/V_{Tr}, given by

$$\frac{I_{of}}{I_{or}} = \left(\frac{V_{Tf}}{V_{Tr}}\right)^a \tag{2}$$

where a is a positive real number. The exponent of this power-law correlation has been suggested as a figure of merit of virtual LO leakage [6]. However, the mechanism behind the existence of power-law correlation is not known. In addition, the validity of power-law exponent as a figure of merit of virtual LO leakage is yet to be justified and verified.

The statistics of dc offset were used to show that a systematic diode mismatch can result from a systematic asymmetric self-heating between the diodes. This systematic diode mismatch correlates with increased virtual LO leakage [8].

The shortcomings in the current knowledge on diode mismatch in APD mixers are apparent. A comprehensive theory relating various aspects of diode mismatch, such as asymmetry in diode parameters, dc offset, and virtual LO leakage, does not exist yet. No clear rules exist on the selection of fabrication process, diode size, and LO pump power for reduced virtual LO leakage. As a result, the yield of MMIC APD mixers has an excessive reliance on the quality of the semiconductor fabrication process. These apparent shortcomings are addressed in this paper through the introduction of two characterization methods and a design approach.

The first characterization method introduced in Section III relies on the statistics of dc offset. The presence of statistical bias in the dc offset indicates a systematic diode mismatch, and a dc offset with a mean of zero indicates a random diode mismatch. The second characterization method introduced in Section IV relies on the power-law correlation expected in the statistics of intrinsic diode parameters for a random diode mismatch and the absence of any correlation for a systematic diode mismatch.

The presence of systematic diode mismatch on top of random diode mismatch correlates with increased virtual LO leakage. Thus, APD circuit sizes that are only subject to random diode mismatch must be chosen over those that are subject to systematic diode mismatch. However, when two APD circuit populations that are subject to comparable degree of random diode mismatch exist, a choice is made between them based on their optimum LO pump power rating, which results in reduced virtual LO leakage. A method of calculating this optimum LO pump power is introduced in Section V. The measurement of dc current–voltage (I/V) characteristics, dc offset, and virtual LO leakage is described in Section VI. Sections VII and VIII contain the results and a discussion. A design approach based on the characterization methods is presented in Section IX.

III. Statistics of DC Offset and Virtual LO Leakage

Diode mismatch is also responsible for the generation of dc offset ($V_{\rm dc}$ in Fig. 1) in an APD mixer [9]. DC offsets are a significant concern in direct conversion systems, where they are often amplified by high-gain dc-coupled amplifiers present in the signal path [9].

The following analysis shows that the statistics of dc offset can be used to classify diode mismatch as either systematic or random. A dc offset with a mean of zero indicates a random diode mismatch, and a statistical bias in the dc-offset statistics indicates a systematic diode mismatch. Furthermore, a dc offset has a linear statistical correlation with virtual LO leakage. This means that the virtual-LO-leakage performance that is inherent to an APD circuit population can be understood directly from the dc-offset statistics.

The current–voltage (I/V) characteristics of the APD circuit in Fig. 1 are given by

$$I(V) = I_{of} e^{\frac{qV}{\eta_f k T_f}} - I_{or} e^{-\frac{qV}{\eta_r k T_r}} \tag{3}$$

where I is the current and V is the applied voltage [6]–[8].

The forward and reverse saturation currents are given by

$$I_{of} = A^{**} T_f^2 W_f e^{-\frac{q\phi_f}{kT_f}} \quad I_{or} = A^{**} T_r^2 W_r e^{-\frac{q\phi_r}{kT_r}} \tag{4}$$

where A^{**} is the modified Richardson constant, W_f and W_r are the forward and reverse junction areas, respectively; and ϕ_f and ϕ_r are the forward and reverse built-in voltages, respectively (see Fig. 1) [8], [10].

Substituting (4) into (3) gives

$$I(V) = A^{**}\left[W_f T_f^2 e^{\frac{q(V-\eta_f\phi_f)}{\eta_f k T_f}} - W_r T_r^2 e^{\frac{-q(V+\eta_r\phi_r)}{\eta_r k T_r}}\right]. \tag{5}$$

A perfectly matched APD circuit contains only odd-degree terms in the Taylor series expansion of its I/V characteristic [6], [15]. When (5) is approximated by a Taylor series, the series also contains even terms due to diode mismatch. These even terms are responsible for the generation of dc offset and virtual LO leakage [6].

For the APD circuit in Fig. 1, the current arising from these even terms is given by

$$i_{2m\omega}(v(t)) = \sum_{m=0}^{r} \frac{1}{(2m)!}\left[\frac{\mathrm{d}^{2m}}{\mathrm{d}V^{2m}} I(V)\right]\Bigg|_{V=0} \times v(t)^{2m} \tag{6}$$

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where m and r are integers and $\mathrm{d}^{2m}/\mathrm{d}V^{2m}I(V)$ is the $2m$th derivative of (5).

The APD circuit's output spectrum contains a dc-offset product and a virtual-LO-leakage product at 2ω. To account for the simultaneous presence of these products, (6) must at least contain terms up to $m = 2$. Hence, (6) can be approximated by

$$i_{2\omega}\left(v(t)\right) = \frac{1}{2!}\left[\frac{\mathrm{d}^2}{\mathrm{d}V^2}I(V)\right]\Bigg|_{V=0} \times v(t)^2. \tag{7}$$

In this instance, a second-order approximation is sufficient to understand the manifestations of random and systematic diode mismatches in the dc-offset statistics and the relationship between dc offset and virtual LO leakage.

Substituting for the second derivative in (7) gives

$$i_{2\omega}\left(v(t)\right) = \frac{A^{**}q^2}{2!k^2}\left[\frac{W_f}{\eta_f^2}e^{\frac{-q\phi_f}{kT_f}} - \frac{W_r}{\eta_r^2}e^{\frac{-q\phi_r}{kT_r}}\right] \times v(t)^2. \tag{8}$$

Since $v(t) = \cos(\omega t)$ (refer to Fig. 1)

$$i_{2\omega}\left(v(t)\right) = \frac{A^{**}q^2}{2!k^2}\left[\frac{W_f}{\eta_f^2}e^{\frac{-q\phi_f}{kT_f}} - \frac{W_r}{\eta_r^2}e^{\frac{-q\phi_r}{kT_r}}\right] \times \frac{1}{2} + \frac{A^{**}q^2}{2!k^2}\left[\frac{W_f}{\eta_f^2}e^{\frac{-q\phi_f}{kT_f}} - \frac{W_r}{\eta_r^2}e^{\frac{-q\phi_r}{kT_r}}\right] \times \frac{1}{2}\cos(2\omega t). \tag{9}$$

The first term of (9) is a current, which corresponds to the dc-offset product in the output spectrum of the APD circuit. The second term of (9) denotes the current corresponding to the virtual LO leakage product.

Subsequently, the dc-offset voltage V_{dc} and the voltage corresponding to the virtual LO leakage product $(V_{2\mathrm{LO}})$ (refer to Fig. 1) are given by

$$V_{\mathrm{dc}} = \frac{A^{**}q^2}{2!k^2}\left[\frac{W_f R_{sf}}{\eta_f^2}e^{\frac{-q\phi_f}{kT_f}} - \frac{W_r R_{sr}}{\eta_r^2}e^{\frac{-q\phi_r}{kT_r}}\right] \times \frac{1}{2} \tag{10}$$

$$V_{2\mathrm{LO}} = \frac{A^{**}q^2}{2!k^2}\left[\frac{W_f R_{sf}}{\eta_f^2}e^{\frac{-q\phi_f}{kT_f}} - \frac{W_r R_{sr}}{\eta_r^2}e^{\frac{-q\phi_r}{kT_r}}\right] \times \frac{\cos(2\omega t)}{2}. \tag{11}$$

A. DC Offset Versus Virtual LO Leakage

Equations (10) and (11) show that the magnitude of the dc-offset voltage is equal to the magnitude of the voltage corresponding to the virtual LO leakage product. This suggests that dc offset and virtual LO leakage have a linear correlation. This is true if the second-order approximation of (6) describes the dc offset and virtual LO leakage in an APD circuit with reasonable degree of accuracy. The linear correlation between V_{dc} and $V_{2\mathrm{LO}}$ is verified by a harmonic-balance (HB) simulation of the APD circuit in Fig. 1, using the ideal diode model and the diode parameters obtained from a population of real APD circuits.

The results of the HB simulation for various LO pump powers are shown in Fig. 2, where dc offset and virtual LO leakage are expressed in decibels relative to the carrier (dBc) and a linear statistical correlation between them is evident. A slight deviation from the statistical linear correlation is present at the higher LO pump powers of 15 and 18 dBm, respectively, owing to the inadequacy of the second-order approximation of (6).

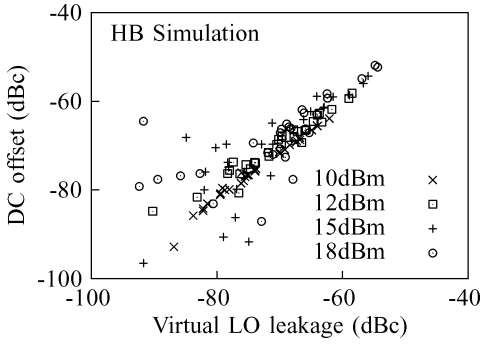

Fig. 2. DC offset and virtual LO leakage are equal in magnitude, as predicted by (9). An HB simulation using the diode parameters of a 25-μm^2 HBT APD circuit population shows a linear statistical correlation.

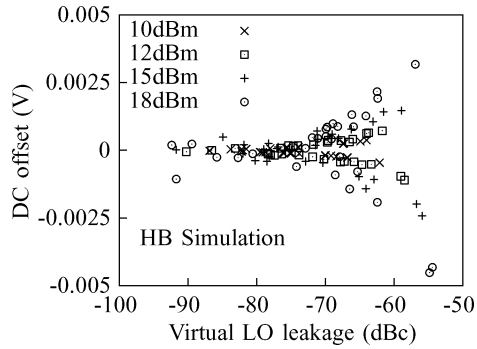

Fig. 3. When dc offset is expressed in volts instead of dBc, the resulting plot does not show a linear relationship between dc offset and virtual LO leakage. However, this type of plot is useful to identify the statistical bias in the dc offset.

If the results of this simulation were plotted such that dc offset is expressed in volts and that virtual LO leakage is in dBc, then the result is a plot shown in Fig. 3. It does not show a statistical linear correlation due to the square-law relationship between voltage and power. Fig. 3 shows the dc offset of a real APD circuit population to have a finite variance and a mean of zero. This suggests that this population of APD circuits exhibit a random diode mismatch [8]. Hence, this type of plot is useful in the characterization of diode mismatch as either random or systematic.

The next section describes how random diode mismatch in an APD circuit population corresponds to a mean of zero in the dc-offset statistics and how systematic diode mismatch corresponds to a statistical bias in the dc-offset statistics.

B. Statistics of DC Offset

Assuming that $T_f = T_r$ in (10) gives

$$V_{\mathrm{dc}} = \frac{A^{**}q^2}{2!k^2}\left[\frac{W_f R_{sf}}{\eta_f^2}e^{\frac{-q\phi_f}{kT}} - \frac{W_r R_{sr}}{\eta_r^2}e^{\frac{-q\phi_r}{kT}}\right] \times \frac{1}{2}. \tag{12}$$

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Equation (12) implies a nonzero dc offset due to the presence of asymmetry in the junction areas, ideality factors, built-in voltages, and series resistances of forward and reverse diodes. The identical forward and reverse junction temperatures in (12) represent the absence of systematic asymmetric self-heating, which can arise from an unavoidable layout asymmetry. The asymmetry in junction areas, ideality factors, built-in voltages, and series resistances represents diode mismatch caused by process variability. As a result, a population of APD circuits described by (12) exhibit a dc offset with a finite variance and a mean of zero, resulting in a plot that is identical to that shown in Fig. 3.

If $T_f = T + \delta T$ and $T_r = T$, where δT is the difference in junction temperatures, then (10) becomes

$$V_{\rm dc} = \frac{A^{**}q^2}{2!k^2}\left[\frac{W_f R_{sf}}{\eta_f^2} e^{\frac{-q\phi_f}{k(T+\delta T)}} - \frac{W_r R_{sr}}{\eta_r^2} e^{\frac{-q\phi_r}{kT}}\right] \times \frac{1}{2}. \quad (13)$$

Equation (13) represents the presence of systematic asymmetric self-heating resulting from the layout asymmetry in an APD circuit. The temperature terms within the exponentials of (13) imply that the asymmetry in junction temperatures dominates over the asymmetry in all other diode parameters. When each of the circuits in an APD circuit population is effected by a systematic asymmetric self-heating owing to layout asymmetry, a statistical bias exists in the dc-offset statistics of the APD circuit population.

Hence, the statistics of dc offset are useful in the identification of systematic effects, such as asymmetric self-heating, and random effects, such as process variability. The next section describes how the statistics of intrinsic diode parameters can be used to characterize diode mismatch.

IV. Statistics of Intrinsic Diode Parameters

The following analysis is used to show that the correlation between I_{of}/I_{or} and V_{Tf}/V_{Tr} can be used to classify diode mismatch as random or systematic.

A power-law correlation is expected between the statistical variation in I_{of}/I_{or} and the statistical variation in V_{Tf}/V_{Tr} when diode mismatch is random. The absence of a power-law correlation indicates the presence of systematic diode mismatch in an APD circuit population.

Consider the asymmetry in saturation currents given by

$$\frac{I_{of}}{I_{or}} = \frac{T_f^2 W_f}{T_r^2 W_r} \frac{e^{\frac{\phi_r}{V_{Tr}}}}{e^{\frac{\phi_f}{V_{Tf}}}}. \quad (14)$$

Assuming that $W_f = W_r$ and applying Stirling's formula (refer to Appendix A) to the exponential terms in (14) give

$$\frac{I_{of}}{I_{or}} = \frac{\left(\frac{\phi_r}{V_{Tr}}\right)^{\frac{\phi_r}{V_{Tr}}}}{\left(\frac{\phi_f}{V_{Tf}}\right)^{\frac{\phi_f}{V_{Tf}}}} \times \frac{\sqrt{2\pi\frac{\phi_r}{V_{Tr}}}}{\sqrt{2\pi\frac{\phi_f}{V_{Tf}}}} \times \frac{\left(\frac{\phi_f}{V_{Tf}}\right)!}{\left(\frac{\phi_r}{V_{Tr}}\right)!} \times \frac{T_f^2}{T_r^2} \quad (15)$$

which, when rearranged and simplified, gives

$$\frac{I_{of}}{I_{or}} = \frac{(\phi_r)^{\frac{\phi_r}{V_{Tr}}}}{(\phi_f)^{\frac{\phi_f}{V_{Tf}}}} \frac{(V_{Tf})^{\frac{\phi_f}{V_{Tf}}}}{(V_{Tr})^{\frac{\phi_r}{V_{Tr}}}} \times \frac{\sqrt{\frac{\phi_r}{V_{Tr}}}}{\sqrt{\frac{\phi_f}{V_{Tf}}}} \times \frac{\left(\frac{\phi_f}{V_{Tf}}\right)!}{\left(\frac{\phi_r}{V_{Tr}}\right)!} \times \frac{T_f^2}{T_r^2}. \quad (16)$$

The ratio of built-in voltage to diode thermal voltage in a diode is much greater than unity. Assume that $\phi_f/V_{Tf} \approx \phi_r/V_{Tr} \approx n$, where $n \gg 1$ gives

$$\frac{I_{of}}{I_{or}} = \left(\frac{V_{Tf}}{V_{Tr}}\right)^n \left(\frac{\phi_r}{\phi_f}\right)^n \times \frac{T_f^2}{T_r^2}. \quad (17)$$

Diode parameters I_{of}, I_{or}, V_{Tf}, and V_{Tr} are representative of the inherent diode asymmetry that is present at zero bias or thermodynamic equilibrium. The junction temperatures are equal at thermodynamic equilibrium. Hence,

$$\frac{I_{of}}{I_{or}} = \left(\frac{V_{Tf}}{V_{Tr}}\right)^n \left(\frac{\phi_r}{\phi_f}\right)^n. \quad (18)$$

It can be shown that (refer to Appendix B)

$$\frac{\phi_r}{\phi_f} \approx \frac{V_{Tf}}{V_{Tr}} \times \frac{T_r}{T_f}. \quad (19)$$

Applying this to (18) gives

$$\frac{I_{of}}{I_{or}} = \left(\frac{V_{Tf}}{V_{Tr}}\right)^{2n} \times \left(\frac{T_r}{T_f}\right)^n. \quad (20)$$

When $T_f = T_r$,

$$\frac{I_{of}}{I_{or}} = \left(\frac{V_{Tf}}{V_{Tr}}\right)^{2n}. \quad (21)$$

This is identical to the relationship that has experimentally been found to exist between the statistical variation in I_{of}/I_{or} and the statistical variation in V_{Tf}/V_{Tr} [6]. It represents the scenario where no asymmetric self-heating is present and diode mismatch is solely due to random process variability. Hence, a power-law correlation should be expected.

Alternatively, the statistical variation in diode parameters across an entire APD circuit population is such that (21) is satisfied for a unique n for an entire population. This makes it a useful method of identifying the presence of random diode mismatch.

If $T_f = T$ and $T_r = T + \delta T$, then (20) becomes

$$\frac{I_{of}}{I_{or}} = \left(\frac{V_{Tf}}{V_{Tr}}\right)^{2n} + \frac{n\delta T}{T}\left(\frac{V_{Tf}}{V_{Tr}}\right)^{2n} \quad (22)$$

when $T \gg \delta T$. When δT is nonnegligible, it introduces a secondary slope in the statistical data of I_{of}/I_{or} and V_{Tf}/V_{Tr}. As this secondary slope becomes more prominent owing to increased systematic effects, power-law correlation ceases. The absence of power-law correlation in the statistics of I_{of}/I_{or} and V_{Tf}/V_{Tr} automatically implies the presence of systematic diode mismatch.

V. Random Diode Mismatch: Reducing Virtual LO Leakage

It is relatively easier to discriminate between APD circuit sizes that are subject to systematic diode mismatch and APD

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circuit sizes that are subject to random diode mismatch based on these characterization methods introduced in Sections III and IV. However, these methods are less useful in discriminating between APD circuit sizes that are only subject to random diode mismatch.

This section introduces a method of discriminating between APD circuit sizes that are affected by random diode mismatch. It relies on an optimum LO voltage calculated for each APD circuit size (using the value of n and the diode parameter statistics). This optimum LO voltage corresponds to reduced virtual LO leakage.

If I_f and I_r are the forward and reverse diode currents, then

$$\frac{I_f(V)}{I_r(V)} = \frac{I_{of}}{I_{or}} \frac{e^{\frac{V}{V_{Tf}}}}{e^{\frac{V}{V_{Tr}}}}. \tag{23}$$

Let

$$\frac{V}{V_{Tf}} \approx \frac{V}{V_{Tr}} \approx m \tag{24}$$

where m is any positive real number that is greater than unity.

This assumption is valid because V_{Tf} and V_{Tr} are small compared to V and their asymmetry is closer to unity for real diodes [7].

Using Stirling's formula (see Appendix A) and (24) in (23) gives

$$\frac{I_f(V)}{I_r(V)} = \frac{I_{of}}{I_{or}} \left(\frac{V_{Tr}}{V_{Tf}}\right)^m. \tag{25}$$

Substituting (21) into (25) results in

$$\frac{I_f(V)}{I_r(V)} = \left(\frac{V_{Tf}}{V_{Tr}}\right)^{2n-m}. \tag{26}$$

When $I_f(V) = I_r(V)$, the diodes are perfectly matched, and no virtual LO leakage is generated in an APD mixer. This condition is satisfied in (26) if $m \approx 2n$ or when

$$\frac{V}{V_T} = \frac{2\phi}{V_T}. \tag{27}$$

This means that the virtual LO leakage arising from process variability (random diode mismatch) is reduced when the APD mixer is operated at an LO voltage, which is twice the diode built-in voltage.

It is important to note that (26) implies that, as the applied voltage is reduced, the asymmetry between diode currents and virtual LO leakage increases. Equation (26) implies a cancellation null. However, this is not strictly true as the current–voltage characteristic is only effective beyond certain voltages, and subsequently, (26) is only valid at those voltages where mixing is due to a nonlinear I/V characteristic. The range of voltages over which (26) is valid corresponds to the LO pump powers required for reasonably efficient mixing.

A. Optimum LO Pump Power

An applied LO voltage of twice the diode built-in voltage is required to improve the statistical yield of APD mixers affected by random diode mismatch.

However, the value of built-in voltage ϕ is unknown. Estimation of ϕ requires measurement of capacitance–voltage characteristics [11]. The statistical variation in the asymmetry of diode built-in voltages also needs to be considered. Owing to the absence of capacitance–voltage data, ϕ is estimated by the following method.

Using the earlier assumption that $\phi_f/V_{Tf} \approx n$,

$$\phi_{f\max} = n\left[\mu(V_{Tf}) + 2\sigma(V_{Tf})\right] \tag{28}$$

$$\phi_{f\min} = n\left[\mu(V_{Tf}) - 2\sigma(V_{Tf})\right] \tag{29}$$

where $\phi_{f\max}$ and $\phi_{f\min}$ denote the ranges of ϕ_f, μ is the mean, and σ is the standard deviation.

Again, using the earlier assumption that $\phi_r/V_{Tr} \approx n$,

$$\phi_{r\max} = n\left[\mu(V_{Tr}) + 2\sigma(V_{Tr})\right] \tag{30}$$

$$\phi_{r\min} = n\left[\mu(V_{Tr}) - 2\sigma(V_{Tr})\right] \tag{31}$$

where $\phi_{r\max}$ and $\phi_{r\min}$ denote the ranges of ϕ_r.

The values of $\mu(V_{Tf})$, $\mu(V_{Tr})$, $\sigma(V_{Tf})$, and $\sigma(V_{Tr})$ are estimated from the statistics of diode parameter V_T, and 2σ is the 95% confidence interval.

Subsequently, the optimum LO pump power typically required to reduce the virtual LO leakage of APD circuits in a population is given by

$$P_{\mathrm{LOopt}}\,(\mathrm{dBm}) = 10\log\left[\frac{(2\phi)^2}{R}\right] + 30 \tag{32}$$

where R is the source resistance. The maximum and minimum values of ϕ_f and ϕ_r when substituted for ϕ in (32) result in a range of values for P_{LOopt}.

TABLE I
APD CIRCUIT POPULATIONS

Process	Diode Size	Samples
HBT	$25\mu\mathrm{m}^2$	30
HBT	$49\mu\mathrm{m}^2$	30
HBT	$100\mu\mathrm{m}^2$	30
HEMT	$0.15\mu\mathrm{m} \times 10\mu\mathrm{m}$	28

TABLE II
FABRICATION PROCESSES

Process	HEMT	HBT
Lithography	E-Beam	Optical
Process f_T	95 GHz	65 GHz
Feature Size	0.15μm	1μm
Geometry	Planar	Vertical
Fingers	2	1

VI. MEASUREMENT

This section describes the measurement of dc current–voltage characteristics, dc offset, and virtual LO leakage in four different APD circuit populations. The four populations are shown in Table I. Three of the APD circuit populations were fabricated on a GaAs heterojunction-bipolar-transistor (HBT) process. The fourth APD circuit population was fabricated on a GaAs high-electron-mobility-transistor (HEMT) process. A comparison of the HEMT and HBT processes is shown in Table II, and the HEMT and HBT APD circuit layouts are shown in Figs. 4 and 5.

In the HBT process, the Schottky diode is formed by the junction between the first interconnect metal and the lightly n-doped collector. The ohmic contact is formed by a collector metal making contact with the heavily n-doped subcollector layer [12]. In the HEMT process, gate metallization was used

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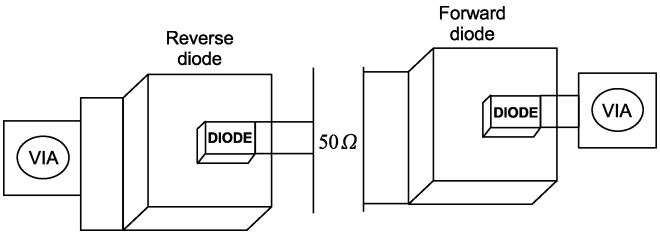

Fig. 4. HBT APD circuit layout.

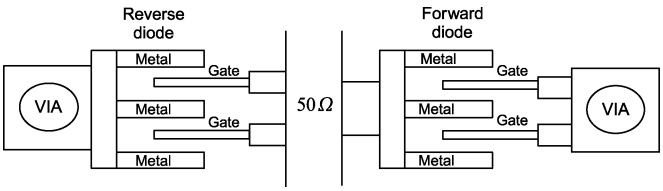

Fig. 5. HEMT APD circuit layout.

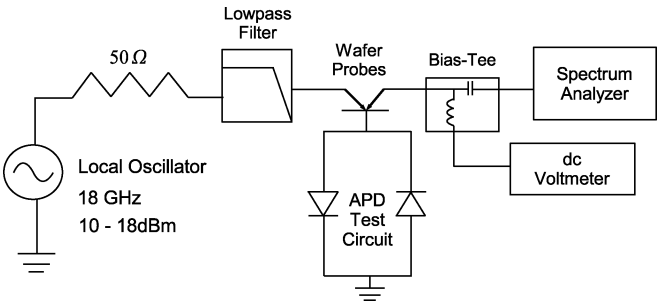

Fig. 6. Setup for measuring dc offset and virtual LO leakage in an APD circuit. It corresponds to the scenario described in Section III and Fig. 1. The low-pass filter is used to minimize second-harmonic leakage from the generator. The dc offset was measured using a two-wire resistance measurement. A two-wire resistance measurement can lead to an artificially low value of dc offset to be measured at the voltmeter. This may explain the discrepancy between the simulated and measured dc offsets of the 25-μm^2 HBT APD circuit population, in Figs. 3 and 7.

to form the Schottky junction, and the source and drain metal contacts were combined to make them ohmic [13].

A. DC Current–Voltage Characteristics

The current-voltage characteristics are measured by applying a dc bias ranging from -1.26 to $+1.26$ V in 30-mV steps at a controlled temperature of 300 K. Diode parameter extraction is used in the extraction of I_{of}, I_{or}, V_{Tf}, V_{Tr}, R_{sf}, and R_{sr} [14], [15].

B. DC Offset and Virtual LO Leakage

The test setup shown in Fig. 6 is excited by a single-tone signal with a frequency of 18 GHz. The resulting virtual LO leakage at 36 GHz and dc offset are measured at drive powers of 10, 12, 15, and 18 dBm.

VII. Results

The 25- and 49-μm^2 HBT APD circuit populations are mainly affected by random diode mismatch. This can be seen from the power-law correlation and the dc offset with a mean value close to zero in Figs. 7 and 8 for the 25-μm^2 HBT population and in Figs. 9 and 10 for the 49-μm^2 HBT population.

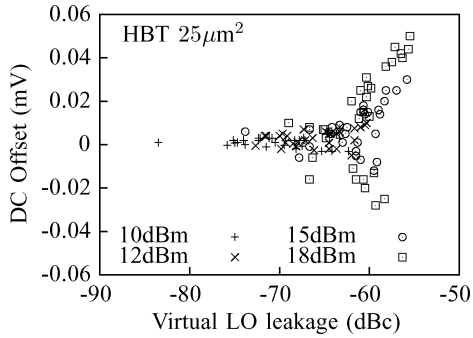

Fig. 7. Zero-mean dc offset indicates random diode mismatch, and a power-law correlation is expected from the statistics of diode parameters. This is confirmed from Fig. 8.

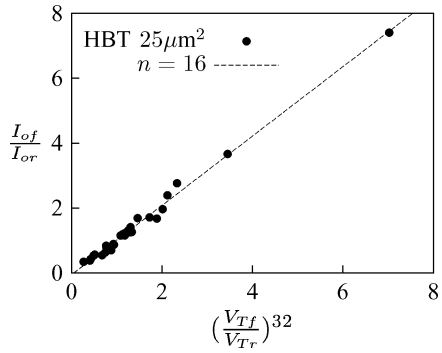

Fig. 8. Line fit has a correlation coefficient of 0.996. The power-law correlation indicates random diode mismatch.

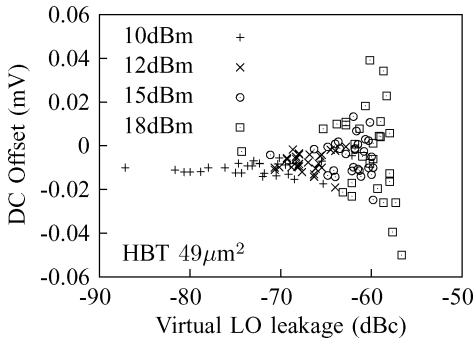

Fig. 9. A dc offset with a mean value close to zero indicates random diode mismatch, and a power-law correlation is expected from the statistics of diode parameters. This is confirmed from Fig. 10.

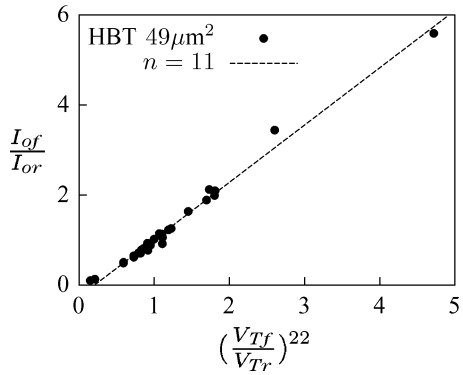

Fig. 10. Line fit has a correlation coefficient of 0.996. The power-law correlation indicates random diode mismatch.

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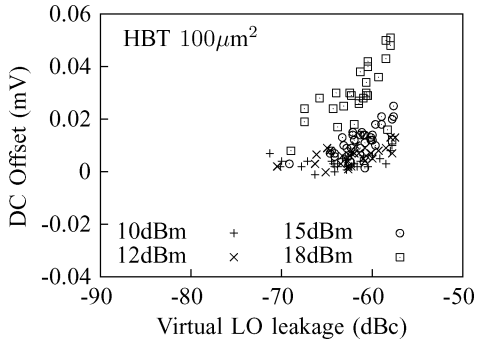

Fig. 11. Statistical bias in the dc offset indicates systematic diode mismatch. Subsequently, a fraction of the circuit population deviate from the power-law correlation in Fig. 12.

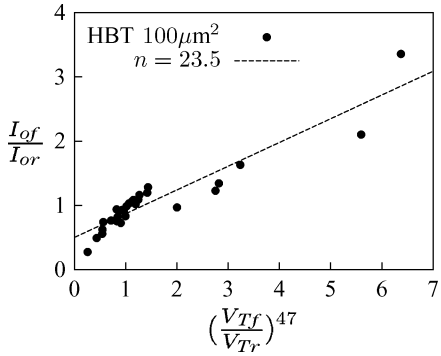

Fig. 12. Correlation coefficient is around 0.936. A slight deviation from the power-law correlation is noticeable.

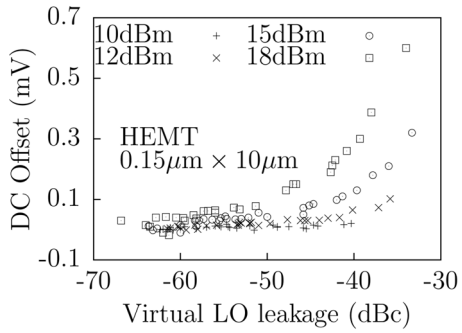

Fig. 13. Statistical bias in the dc offset indicates systematic diode mismatch.

Systematic diode mismatch is found to exist in the 100-μm^2 HBT APD circuit population. This can be seen in Figs. 11 and 12. The 0.15 μm $\times$ 10 μm HEMT APD circuit population is also affected by systematic diode mismatch, which is evident from the statistical bias in the dc offset in Fig. 13 and the absence of power-law correlation in Fig. 14.

VIII. Discussion

The dc-offset and virtual-LO-leakage products were shown to have a statistical linear correlation in Section III. This is substantiated by the simulation results of the 25-μm^2 HBT APD circuit population in Fig. 2.

The simulated dc offset (in volts) plotted against the simulated virtual LO leakage (in dBc) in Fig. 3 can be compared with the plot in Fig. 7. Both plots show that the 25-μm^2 HBT APD circuit population has a dc offset with a finite variance and a mean of zero. The plots also have identical simulated and measured virtual LO leakages. However, the simulated dc offset in Fig. 3 is clearly different from the measured dc offset in Fig. 7.

Since the dc offset and virtual LO leakage have a linear statistical correlation, an agreement between the simulated and measured virtual LO leakages must also translate to an agreement between the simulated and measured dc offsets. There is only one reason for the discrepancy between the simulated dc offset in Fig. 3 and the measured dc offset in Fig. 7.

First, the dc-offset voltages in APD circuits are small in magnitude to begin with. When the dc offset is measured through a two-wire resistance measurement (refer to Fig. 6), it can lead to artificially low voltage to be measured at the voltmeter. This would also explain why the dc offset measured in volts for each APD circuit population (refer to Figs. 7, 9, 11, and 13) is too low to exhibit a linear correlation with the measured virtual LO leakage values. An accurate measurement of dc offset requires a kelvin four-wire resistance measurement.

However, this discrepancy does not affect either the characterization of diode mismatch or the comparison of the extent of diode mismatch in various APD circuit sizes.

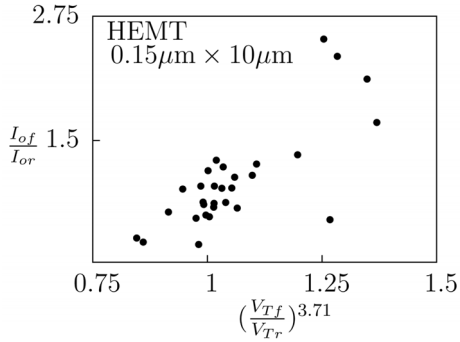

Fig. 14. Best correlation coefficient (0.74) is achieved when the asymmetry in diode thermal voltage is raised to the power of 3.71. However, no power-law correlation is present due to systematic diode mismatch.

IX. Design Approach: Improving Yield

This section introduces a design approach for improved APD mixer yield based on the characterization methods and the concept of optimum LO pump power. The approach involves characterization of the diode mismatch in each APD circuit size under consideration and selection of only those APD circuit sizes that are only subject to random diode mismatch.

When only random diode mismatch is present in an APD circuit population, the virtual LO leakage that is inherent to an APD circuit size is reduced by operating the APD mixer closer to the optimum LO pump power. This optimum LO pump power is calculated from the exponent of the statistical power-law correlation and varies with diode size. The diode size with the lowest n and lowest $P_{\mathrm{LO\,opt}}$ is chosen. A stepwise description of this approach are outlined as follows.

1) Fabricate APD circuits of different sizes using a semiconductor fabrication process.

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TABLE III
PARAMETERS OF APD CIRCUIT POPULATIONS BASED ON THE CHARACTERIZATION METHODS

Process	Diode Size	Statistical Bias	n	P_{LOopt} (dBm)
HBT	$25\mu\text{m}^2$	No	16	$11.5-12.5$
HBT	$49\mu\text{m}^2$	No	11	$8.4-9$
HBT	$100\mu\text{m}^2$	Yes	23.5	$15-15.5$
HEMT	$0.15\mu\text{m}\times 10\mu\text{m}$	Yes	–	–

2) Measure the dc offset of each APD circuit in a population (use kelvin four-wire measurement in the test setup of Fig. 6).
3) Eliminate populations with statistical bias in the dc offset.
4) Consider populations in which the dc offset has a mean of zero.
5) If the dc-offset statistics of the diode sizes under comparison are markedly different, then selection is made directly from the dc-offset statistics. However, if there is little distinction, then power-law characterization is necessary.
6) Now, measure the dc I/V characteristics of the APD circuit populations.
7) Identify n and calculate P_{LOopt} for each of these APD circuit populations.
8) Select the APD circuit size with the lowest values of n and P_{LOopt}.
9) Use HB to verify the conversion gain and linearity of the APD mixer using the selected diode size over the frequency band of interest. Process variability has a relatively minor influence on conversion gain and linearity when compared to diode mismatch and virtual LO leakage.
10) Design the APD mixer using the selected diode size for improved circuit yield.

A. Verification

The design approach introduced in Section IX is verified using the data obtained from the four APD circuit populations (see Table I). The parameters obtained from the statistics of the APD circuit populations are shown in Table III.

The design approach introduced in this section automatically disqualifies the 100-μm^2 HBT APD circuit and the 0.15 μm $\times$ 10 μm HEMT APD circuit populations owing to the statistical bias that is evident in their respective dc-offset statistics. The remaining two HBT APD circuit populations of 25 and 49 μm^2 have a dc offset with a mean of zero, and it is difficult to distinguish between these two circuit sizes based on their dc-offset statistics.

However, both of these circuit sizes have different values of n and P_{LOopt}. Thus, a choice can be made between these two APD circuit sizes. The 49-μm^2 diode size is chosen for the APD mixer owing to its lower values of n and P_{LOopt}.

The mean values of the measured virtual LO leakage of each of the APD circuit populations are plotted as a function of LO pump power in Fig. 15. These results confirm that the 49-μm^2 diode size is the appropriate choice if the APD mixer were to be operated at an LO pump power of 10 dBm. This compares favorably with the P_{LOopt} values calculated in Table III. The measured data are not available below the 10-dBm LO pump power. It should be noted that the 49-μm^2 diode has considerable variance at P_{LOopt}, as shown by the error bars. However, larger sample sizes are required to understand the issue of variance.

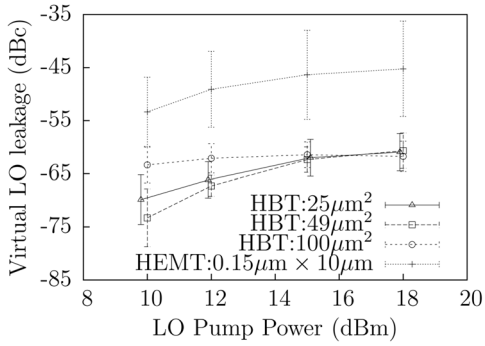

Fig. 15. Mean value of virtual LO leakage as a function of LO pump power for various APD circuit sizes. The mean values are obtained from the measurement of 30 samples in each APD circuit population. The error bars represent the 95% confidence intervals. The 49-μm^2 HBT APD circuit size offers the best statistical virtual-LO-leakage performance at an LO pump power of 10 dBm, followed by the 25-μm^2 HBT APD circuit size. A larger sample size is required to get an improved estimate of the variance.

The next best diode size is 25 μm^2, which appears to have the best mean virtual LO leakage between 10 and 12 dBm in Fig. 15. This compares favorably with the P_{LOopt} values calculated in Table III. This diode size also shows considerable variance at an LO pump power of 10 dBm.

The next best diode size is 100 μm^2, which is subject to systematic diode mismatch. However, the extent of systematic diode mismatch is small enough to allow the presence of statistical power-law correlation and to enable the calculation of n. The value of n for this diode size is considerably larger, indicating increased virtual LO leakage. The value of P_{LOopt} for the 100-μm^2 APD circuit is 15 dBm in Table III. The mean value of the measured virtual LO leakage does not appear to contradict with P_{LOopt}, as the mean virtual LO leakage is constant at all LO pump powers in Fig. 15.

The 0.15 $\times$ 10 μm^2 HEMT APD circuit population has the highest mean value for the measured virtual LO leakage at all LO pump powers by a considerable margin, owing to the considerable systematic diode mismatch arising from the layout asymmetry of the HEMT structure (see Fig. 5). Hence, this fabrication process and diode size are ill suited in applications where virtual LO leakage and component cost are critical.

This analysis does not take into account the relative conversion-gain performance of each of the diode sizes. In the case of statistical yield, there is considerable reason to expect process variability to have significantly lesser effect on conversion gain than virtual LO leakage. However, factors such as the magnitude of diode series resistance and zero-bias junction capacitance, which vary with diode size, determine the conversion gain in an APD mixer. Conversion gain is affected by the absolute values of these parameters, whereas virtual LO leakage is affected by their relative differences. It is maybe because these two issues are unrelated. Further investigation is required to understand the tradeoffs, if any.

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X. Conclusion

A design approach based on the characterization of systematic and random diode mismatches can be used to improve the virtual-LO-leakage performance of APD mixers. It relies on the statistics of diode parameters and dc offset to identify the diode size and LO pump power that result in improved APD mixer yield.

Appendix A
Stirling's Formula

Stirling's formula is used to calculate the factorial of a number [16], [17]. It is given by

$$a! \approx a^a e^{-a}\sqrt{2\pi a}. \tag{33}$$

It can be rearranged as

$$e^a \approx \frac{a^{a+0.5}\sqrt{2\pi}}{a!}. \tag{34}$$

Equation (34) implies that

$$e^x\big|_{x=a} \approx \left.\frac{x^{a+0.5}}{x!}\sqrt{2\pi}\right|_{x=a}. \tag{35}$$

Equation (35) implies that an exponential function e^x can be approximated by $a + 0.5$th power term when $x = a$.

Appendix B
Relationship Between ϕ_f/ϕ_r and V_{Tf}/V_{Tr}

The diode built-in voltage ϕ varies with the applied voltage [10], [18]. This variation is defined by

$$\eta = \frac{1}{1 - \frac{\mathrm{d}\phi}{\mathrm{d}V}}. \tag{36}$$

The solution of (36) for an initial condition of $V = 0$ gives

$$\phi(V) = \left(1 - \frac{1}{\eta}\right)V + \phi \tag{37}$$

where ϕ is the built-in voltage under equilibrium conditions.

The variation in the built-in voltage of diodes marked forward and reverse (refer to Fig. 1) is given by

$$\phi_f(V) = \left(1 - \frac{1}{\eta_f}\right)V + \phi_f \tag{38}$$

$$\phi_r(V) = \left(1 - \frac{1}{\eta_r}\right)V + \phi_r. \tag{39}$$

Then

$$\frac{\phi_f(V)}{\phi_r(V)} = \frac{\left(1 - \frac{1}{\eta_f}\right)V + \phi_f}{\left(1 - \frac{1}{\eta_r}\right)V + \phi_r}. \tag{40}$$

Substituting $\eta_f = qV_{Tf}/kT_f$ and $\eta_r = qV_{Tr}/kT_r$,

$$\frac{\phi_f(V)}{\phi_r(V)} = \frac{qV_{Tf}(V + \phi_f) - kT_fV}{qV_{Tr}(V + \phi_r) - kT_rV} \times \frac{T_r}{T_f} \times \frac{\eta_r}{\eta_f}. \tag{41}$$

However, $qV_{Tf} \approx qV_{Tr} \approx 10^{-21}$ and

$$\frac{\phi_f(V)}{\phi_r(V)} = \frac{-kVT_f}{-kVT_r} \times \frac{T_r}{T_f} \times \frac{\eta_r}{\eta_f}. \tag{42}$$

Equation (42) shows that the zero-bias asymmetry in built-in voltages is independent of the applied voltage, which is to be expected.

Simplifying (42) and substituting for η_f and η_r give

$$\frac{\phi_f(V)}{\phi_r(V)} = \frac{\eta_r}{\eta_f} = \frac{qV_{Tr}}{kT_r} \times \frac{kT_f}{qV_{Tf}}. \tag{43}$$

Then

$$\frac{\phi_f}{\phi_r} = \frac{V_{Tr}}{V_{Tf}} \times \frac{T_f}{T_r}. \tag{44}$$

Alternatively,

$$\frac{\phi_r}{\phi_f} = \frac{V_{Tf}}{V_{Tr}} \times \frac{T_r}{T_f}. \tag{45}$$

Acknowledgment

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