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Electrothermal Gate and Channel Breakdown Model for Prediction of Power and Efficiency in FET Amplifiers

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Abstract— **A model of gate-junction leakage and impact ionization is used to predict catastrophic junction- and avalanche-breakdown mechanisms in a FET. It is shown that low-power dc measurements can be used to characterize breakdown and that the model correctly extrapolates to regions outside the safe-operating-area. When included in a large-signal FET model with dynamic calculation of junction temperature, the output power, power-added efficiency (PAE) and peak PAE of a common-source amplifier are well predicted.**

Index Terms— **Avalanche breakdown, Electrothermal effects, Impact ionization, Microwave FET power amplifiers, Semiconductor device breakdown**

I. INTRODUCTION

The output of power amplifiers using a field effect transistor (FET) operating over the full extent of its characteristics is limited by the knee region and by breakdown at high drain potentials. Given that there is no restriction on the choice of drain bias, these limits determine the onset of gain compression and maximum achievable output power.

Using a FET at best efficiency and full power often requires operation at the limit set by breakdown mechanisms. Measured power-added efficiency (PAE) is reduced as output power is further increased. However, simulations tend to predict a continuing increase in efficiency. The problem in determining the breakdown limit of the FET is that it varies with temperature, and hence operating power. It is also accompanied by catastrophic failure, so it is inherently impossible to measure and any simple implementation in a circuit simulator leads to numerical instability.

This paper examines the prediction of breakdown mechanisms from leakage currents observable in regions well-before catastrophic breakdown. A model of gate and drain currents due to avalanche and gate-junction breakdown mechanisms is presented in Section II. In Section III simulations with a FET description that incorporates this model are compared with measurement of efficiency and self-biasing behavior. The influence of the breakdown mechanisms is investigated in Section IV and their significance is demonstrated. The conclusion drawn in Section V is that the breakdown model correctly extrapolates to regions outside the safe-operating-area. This is important for power and efficiency predictions.

II. DRAIN CURRENT BREAKDOWN

Before the occurrence of catastrophic breakdown there is a measurable contribution to gate and drain currents from breakdown mechanisms that impose limits on dynamic load lines. One breakdown mechanism is an increase in gate-junction current at excessive reverse bias. Another breakdown mechanism is excessive channel current caused by an avalanche process induced by high electric fields. The dominance of either mechanism is determined by their temperature and terminal-potential dependencies.

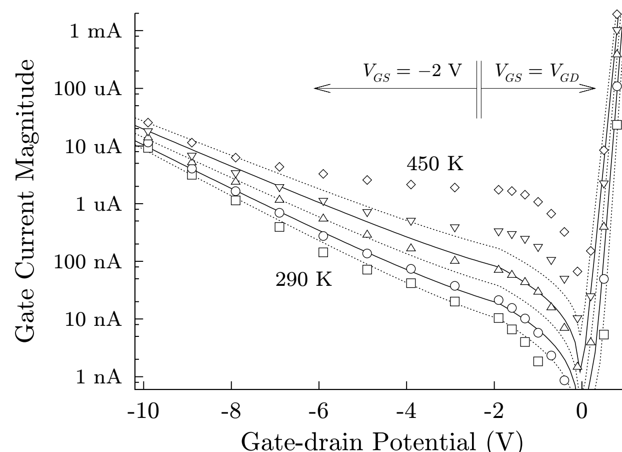

Fig. 1. Measured (points) and calculated (lines) gate currents versus gate-drain potential, V_{GD}, of a 240×0.5μm Agilent pHEMT (on-wafer) with ambient temperatures at 290, 330, 370, 410, and 450 K as the parameter. The calculations used (1) with forward current parameters (at $T_n = 300$ K) $I_0 = 50$ fA, $N_0 = 1.6$, $E_0 = 0.8$ V, and reverse current parameters $I_1 = -130$ pA, $N_1 = -37$, $E_1 = 0.34$ V, $I_2 = -1.4$ nA, $N_2 = -48$, and $E_2 = 0.08$ V. The gate-source potential is fixed or varied as annotated.

A. Gate-junction Breakdown

Reverse gate-drain potential induces a gate-junction reverse-leakage current in a forward-mode common-source FET. The gate current increases with junction temperature and reverse gate-drain potential. Catastrophic breakdown is often described as a rapid increase in leakage current at a critical potential that follows a multiplier or power-law function [1]. However, at high potentials, measured gate currents follow an exponential function similar to that used for the forward current in the standard diode model as shown in Fig. 1.

The gate-drain current model proposed here is a sum of three exponential functions with temperature dependence:

$$i_{GD} = \sum_{i=0}^{2} I_i \, A(E_i, T) \left[\exp\left(\frac{q}{N_i \, k \, T} \, v_{GD} \right) - 1 \right] \qquad (1)$$

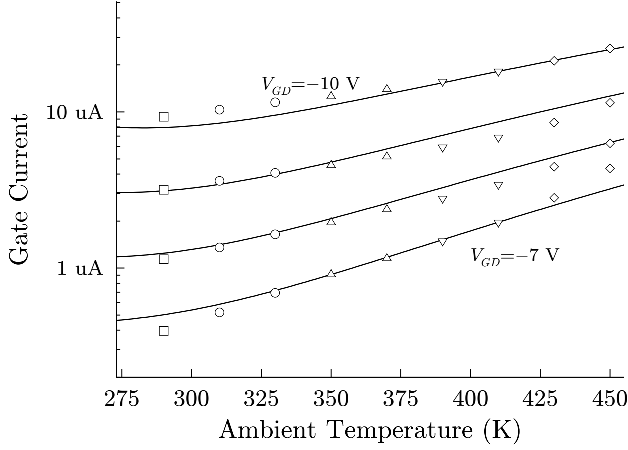

Fig. 2. A subset of measured (points) and simulated (lines) gate currents from Fig. 1 shown versus temperature. Gate-drain potentials from –10 to –7 V in 1V steps is the parameter ($V_{GS} = -2$ V).

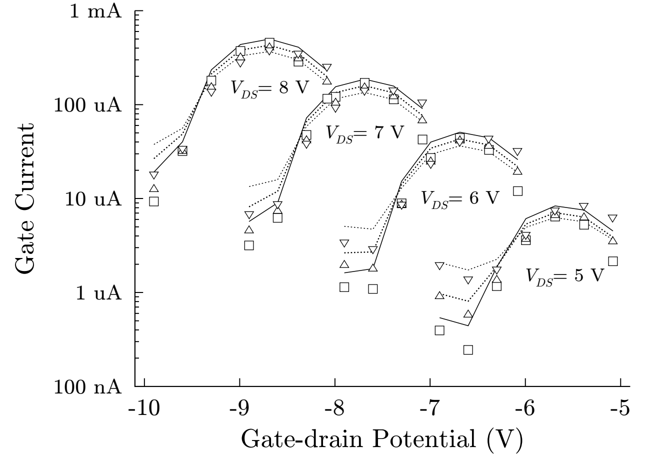

Fig. 3. Measured (points) and simulated (lines) gate currents versus gate-drain potential at four drain-source potentials as annotated. Temperatures are at 290 K (solid line), 350 K, and 410 K. The gate potential is swept to produce each line. Simulations are the sum of (2) with $A_I = 25$, $B_I = 53$ V, $B_T = 0.00015$ K^{-1}, $\phi_B = 0.7$ V, and $\sigma = 2$ V, and (1) with the same parameters used for Fig. 1.

where

$$A(E_i, T) = \left(\frac{T}{T_n}\right)^2 \exp\left[\frac{q\,E_i}{k}\left(\frac{1}{T_n} - \frac{1}{T}\right)\right].$$

The first term ($i = 0$) is the standard forward-biased diode function. The terms $N_0 > 0$ and $A_0 > 0$ are set to fit the forward gate current region ($V_{GD} > 0$). The remaining terms ($i > 0$) are used to describe the reverse gate current. The parameters $N_{1,2} < 0$ and $A_{1,2} < 0$ are set to fit breakdown current at high gate-drain potential. That is, the reverse-leakage current is described by two paralleled ideal diodes connected in reverse.

This model is shown in Fig. 1 for two measurement regions. One is at pinch-off with substantial reverse gate-drain potential. The second is at zero drain potential, so that gate-drain and gate-source potentials are equal. For the latter region the simulation includes a gate-source current i_{GS}, which is also given by (1) in terms of v_{GS}.

At low drain potentials, V_{GD} between –6 and 0 V, there are current spreading and other leakage currents. These are not significant to the breakdown mechanism at high potentials, so have not been accounted for in this work.

Temperature dependence of each current contribution is described by an Arrhenious relationship set by an activation energy E_i. A single activation energy, E_0, describes the forward current well. However, to accommodate the dependency shown in Fig. 2, two terms with different activation energies, E_1 and E_2, are included in (1). This describes the dependency in the high-potential region, over a typical operating range adequately. An accurate identification of the activation energies requires measurements over a wider range of temperature.

B. Avalanche Breakdown

Impact ionization occurs in the channel at a rate determined by the drain-source electric field. This adds to the drain's electron current and produces an opposing hole current toward the source [2]. An avalanche breakdown can occur because the additional current is proportional to the total current, which includes the additional current.

A contribution to gate current is observed when holes tunnel to the gate [3]. This is well modeled by:

$$i_G = i_{DS} \cdot A_I \exp\left(-\frac{B(T)}{v_{DS}}\right) \cdot \exp\left(\frac{\sigma}{v_{GS} - \phi_B}\right) \quad (2)$$

where

$$B(T) = B_I\,[1 + B_T\,(T - T_n)]\,.$$

The parameters A_I and B_I [V] characterize the impact ionization rate [1] with a thermal coefficient B_T [K^{-1}] [4]. The parameter σ [V] sets the hole tunneling probability, which is a function of gate-source potential and the junction's built-in potential ϕ_B [V].

Figure 3 shows an application of (2) to model measured gate current in regions of impact ionization. Each curve in the graph shows an initial increase in gate current proportional to the increase in drain current that arises as the gate potential is increased. As the gate potential increases further, there is a reduction in tunneling probability that reduces the current. Note that although temperature dependence of tunneling has not been addressed, it only affects gate current and not the drain-source breakdown.

C. Simulator Implementation

The breakdown elements have been added to a complete transistor model that provides for interaction with junction temperature and charge trapping [5]. The model dynamically calculates junction temperature with an electro-thermal equivalent of thermal resistance and heat capacity [6]. This facilitates simulation of temperature change as bias conditions vary with signal power.

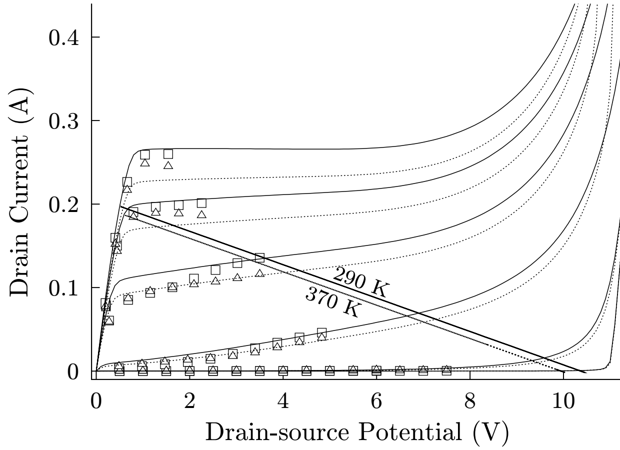

Fig. 4. Dynamic load line for a 1-GHz input at 9 dBm (1 dB compression point) overlaid on simulated characteristics with V_{GS} from –2.4 to 0.6 V in 0.6V steps as the parameter. Solid lines are for 290 K and dotted lines are for 370 K. Measured dc characteristics of a 600×0.5μm Agilent pHEMT (on-wafer) at 290 K (□) and 370 K (◇) are shown for reference. For $T_n = 300$ K the forward current parameters are $I_0 = 0.082$ fA, $N_0 = 1.3$, $E_0 = 0.6$ V and the reverse current parameters are $I_1 = -50$ fA, $N_1 = -27$, $E_1 = 1.1$ V, and $I_2 = 0$ A. The thermal resistance, used to determine T, is 50 K/W.

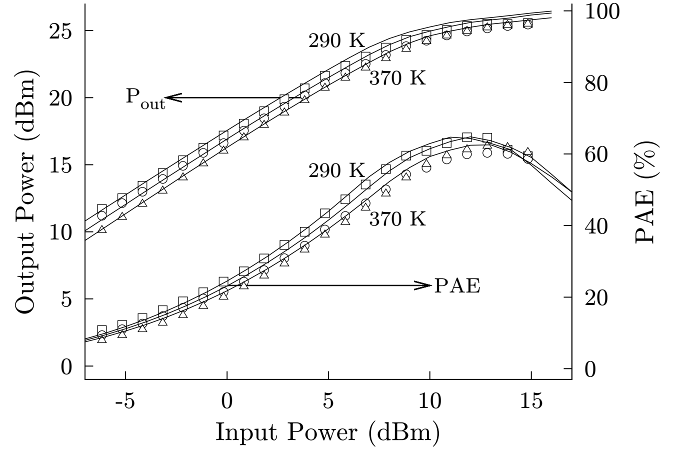

Fig. 5. Power-sweep measurements at 290 (□), 330 (△), and 370 K (◇) and corresponding simulations. Shown are gain and PAE for the HEMT in Fig. 4 operating in common-source configuration at a quiescent point of $V_{DS} = 6.5$ V and $V_{GS} = -1.5$ V. The parameters are the same as for Fig. 4.

The simulated characteristics of a HEMT with breakdown are shown in Fig. 4. Although the simulation extrapolates beyond the safe-operating-area, there is a high degree of confidence in the prediction for two reasons. First, the breakdown model is based on measured data similar to that of Figs 1 and 3, which establishes its bias and temperature dependence. Second, the junction temperature is calculated dynamically, so self-heating is accounted for. It is interesting to note that impact ionization reduces with temperature whereas junction breakdown increases with temperature [7]. This implies that although impact ionization can cause an avalanche breakdown, it is thermally stable whereas junction breakdown can undergo thermal runaway.

Numerical stability with respect to avalanche and thermal runaway is achieved by imposing a limit on temperature response to a sensible range and by redefining the exponential function to limit the maximum current. This allows simulation of avalanche breakdown and thermal runaway to excessive but not numerically-extreme limits, as shown in Fig. 4. These limits smoothly constrain the exponential functions, which gives improved convergence at moderate bias conditions.

The key aspect of the basic transistor model is dynamic calculation of temperature. With this the effect of breakdown on high-power operation can be illustrated. The details of the transistor model are a secondary consideration because adding the breakdown and temperature model to other descriptions would also show the same trends that are investigated here.

III. High-power Operation

Power sweeps were carried out to investigate the influence of breakdown on power and efficiency of the transistor illustrated in Fig. 4 operating in common-source configuration. The device size was designed to suite a 50Ω load line, so that direct on-wafer measurements could be carried out without interposing matching networks. A relatively low frequency of 1 GHz was used to suite the resistive load. This allowed straightforward calibration of power levels at the gate and drain probe pads, which were used as the reference plane for results shown here.

A power meter was used to calibrate the signal source, feed losses, and the spectrum analyzer. A 5W, 30dB attenuator was the primary load, which protected the spectrum analyzer. The wafer was mounted on a metal backplane and measurements were made on a temperature-controlled probe station. Several quiescent points in class A, AB, and C ranging from 4 to 8 V were investigated. All were well described by the breakdown model and exhibited varying degrees of temperature and breakdown dependence. A class-AB point that is limited by breakdown and demonstrates some temperature dependency has been chosen for the following discussion of high-power operation.

A. Power-sweep Measurements

Figure 5 shows measured and simulated output power versus input power at the gate pad. Output power is seen to reduce with temperature, which is expected because drain current reduces. The 1-dB compression point occurs at about 9 dBm input and the load line for this point is shown in Fig. 4.

Power-added efficiency (PAE) is also shown in Fig. 5 and is seen to reduce with temperature. When temperature is increased, the peak efficiency occurs at reduced input levels. Beyond the peak there is a cross-over effect and efficiency increases with temperature. Breakdown mechanisms are significant in this highly-compressed region.

Figure 6 shows measured and simulated bias currents versus input power at the gate pad. There is a significant bias shift

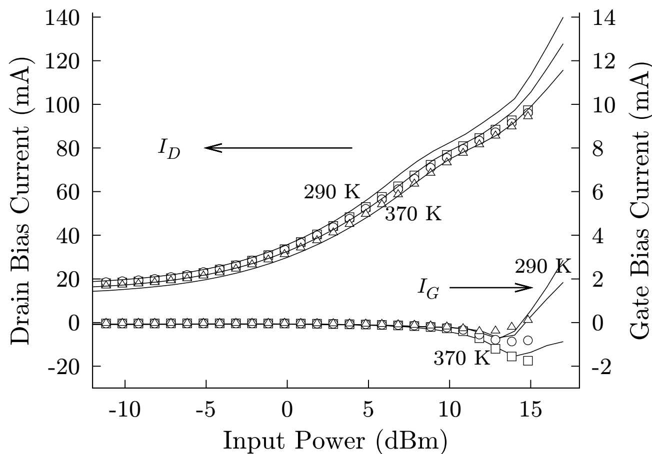

Fig. 6. Power-sweep measurements of bias currents at 290 (□), 330 (△), and 370 K (◇) and corresponding simulations for the HEMT in Figs 4 and 5.

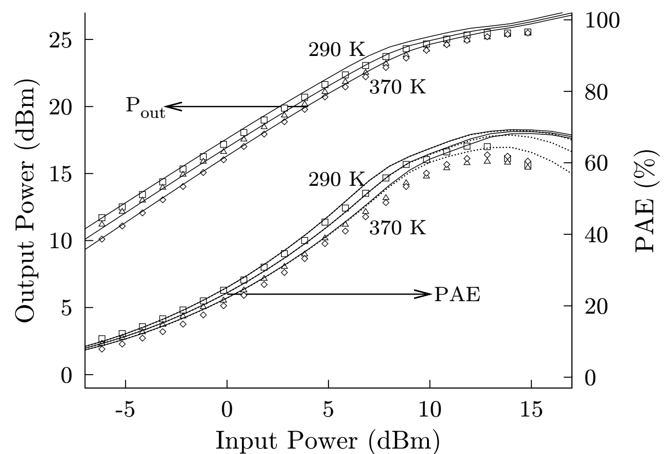

Fig. 7. Power-sweep measurements at 290 (□), 330 (△), and 370 K (◇) and corresponding simulations. Shown are gain and PAE measurements from Fig. 5. The simulations are with impact ionization disabled (dashed lines) and with both impact ionization and gate-junction breakdown disabled (solid lines).

from 10% to 50% I_{DSS} as power is increased. The rate of increase of drain current slows at around 8 dBm input level when gain compression occurs. It increases rapidly for input levels above 14 dBm when significant breakdown is induced.

The gate's bias current, shown in Fig. 6, is a clear indicator of both breakdown mechanisms and forward gate-junction conduction. The simulation of these is an extrapolation by the model that was fitted to measured data as discussed in Section II-C. The quality of the prediction, shown in Figs 5 and 6, across temperature and power level is quite good and indicates that the breakdown effects are being well modeled.

IV. Investigative Simulations

The influence of gate and drain breakdown currents on gain and efficiency can be investigated by disabling these in simulations. Figure 7 shows simulations with only impact ionization disabled and with both impact ionization and gate-junction breakdown disabled. Without impact ionization, the simulations overestimate efficiency and the input power at peak PAE, as shown by the dashed lines in Fig. 7. In the highly-compressed region, efficiency increases with temperature incorrectly and the cross-over effect in Fig. 5 is lost. There is also a reduced negative excursion in the gate's bias current.

Without junction breakdown and impact ionization, the simulations fail to predict PAE peaking or temperature dependence in the highly-compressed region. In this simulation the gain compression is set by power-rail limits and the forward-gate diode current. The efficiency is significantly overestimated because breakdown occurs at lower power limits.

V. Conclusion

An accurate breakdown description is necessary to predict gain compression, PAE, and PAE peaking. A model that includes gate-junction breakdown and impact ionization that accomplishes this has been presented. By describing leakage currents at moderate bias conditions, the model can be characterized without catastrophic measurements. The ability to correctly extrapolate to regions outside the safe-operating-area has been demonstrated by successful power and efficiency predictions. The implementation of the model in a circuit simulator now enables investigation of breakdown in designs and identification of the influence of breakdown on efficiency and dynamic load lines.

Acknowledgements

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