Scalable HEMT Model for Small Signal Operations

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***Abstract*— The aim of this work is to develop a scalable small signal HEMT model. We propose a general intrinsic model "unit cell" to build larger transistor devices according to our need and model the metal according to individual geometry using a lumped element network. The challenge we address is extraction of this network from measurement. The parameters of the intrinsic part of the transistor have been extracted from different size of transistors and scaling rule applied to the unit cell. We used MathCAD worksheet to de-embed the TriQuint transistor parameters. Multiple cells are used to build larger devices and we showed that coupling between cells with lumped element affects the S-parameter responses. The interconnection with lumped elements was varied according to the need to fit with larger device responses.**

1 INTRODUCTION

Generally a FET device model is composed of the intrinsic and extrinsic networks. Intrinsic device parameters are bias dependent and linearly scalable with the total gate periphery of the device. The extrinsic network is bias independent [1] and depends on physical layout of the device e.g. interconnection, electrode structures and probe pads.

The issue of model scalability is of prime importance, especially to design engineers working in MMIC design foundries, who need to have more flexibility and confidence to use a wide range of device sizes in their design. Number of scaling rules has been proposed so far, but these don't consider coupling between metal interconnection correctly. Scaling large device from small cell is a useful technique for the engineers [2-3].

Linear scaling rules are widely used for the intrinsic device up to relatively high frequencies and these rules work fine in most of the cases. But the problem is, there is no straight forward rule for scaling extrinsic devices, while the overall quality of the device depends on the extrinsic values. Some researchers employ a Full-Wave Electro-Magnetic (FW-EM) simulation to extract layout dependent extrinsic parameters [4]. A geometrical structure based extrinsic modelling has been proposed [5] which considers number of gate fingers and spacing distance of inner coplanner wave-guide. They have tried to establish some scaling factor, determined by measuring a number of devices.

In this work we proposed distributed PHEMT modelling technique using a pre-determined intrinsic model and only varying the extrinsic network elements. We applied linear scaling rule in to some of the extrinsic parameters and optimized the values of other parameters by Electromagnetic Simulations. We created a 2x25um device, which consists of intrinsic and extrinsic, we call it Unit Cell (UC), and then cascaded four cells using an assembling network to get the full response of a 2x100um device. Section 2 describes Distributed model, Section 3 Verification of the model, Section 4 Discussion and, finally Conclusion.

2. DISTRIBUTED MODEL

Measured data from a TriQuint Semiconductor 2x100um PHEMT transistor was taken using Vector Network Analyzer (VNA) up to 50GHz. A robust extraction method is explained in [6] and the algorithm is readily available in our lab, and used the algorithm in MathCAD [7] to de-embed the intrinsic and extrinsic parameters. Fig.1 shows the extracted model of a 2x100um device. We used the same model to create the UC and Fig.2 shows the geometrical structure of a 2x100um transistor.

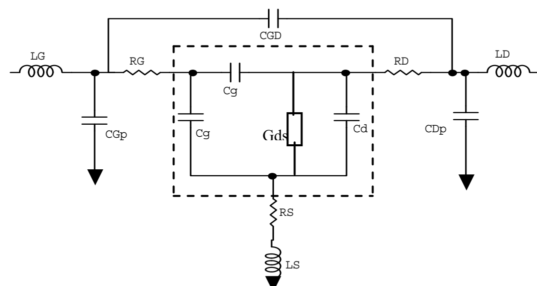

Fig. 1.Extracted model of a 2x100um transistor-intrinsic parameters are inside the doted box

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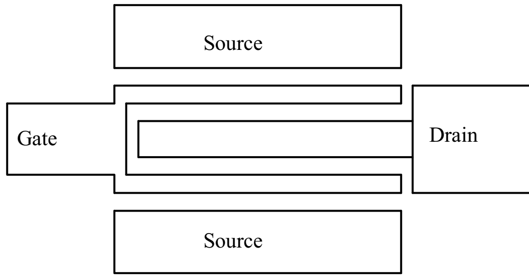

Fig. 2.Geometrical structure of a 2x100um transistor

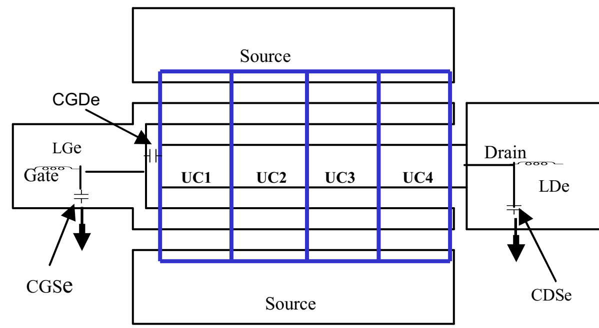

Fig. 3: Slicing the 2x100um transistor into four unit cells

2.1 Unit Cell

Applying the typical linear scaling rule on the intrinsic parameters of 2x100um we determined the values for the proposed UC as in Table.1. We also applied linear scaling rules to LS, RS and RD for UC; these parameters are presented in Table.2 with other parameters that will be discussed later.

Table.1 2x25um parameters, these values are ¼ of 2x100um transistor's extrinsic

Intrinsic of UC	
Cgs	58.552 fF
Cgd	5.5675 fF
Cds	0
Gm	0.038694 ohm
Gds	0.001571 sec
Xds_gs	0.004789

The 2x100um transistor was then sliced into four pieces as shown in Fig.3. In our model we consider λg/25 (λg is the electrical wavelength) dimension over which the distributed model will be considered and for this reason we created four cells (active slides). The slices are marked as UC1, UC2, UC3 and UC4.

Each UC is a 2x25um transistor, which is placed in the four-port network as shown in Fig.4. Inside the network the box represents the intrinsic parameter values. Ports 1, 4 are either end of gate and ports 2, 3 are either end of drain side. The source of each UC is connected to the ground. The extrinsic parameters of each unit cell U are presented in Table.2. Since four cells are going to be connected, RS and LS, RD, CGS, CGD, CDS are going to be parallel in their respective cells. We took RS, LS and RD four times of the 2x100um transistor's value. While LG, RG, LD will be in series in the respective cells. Optimizing LG, RG, LD, CGS and CDS we found distributed values for them.

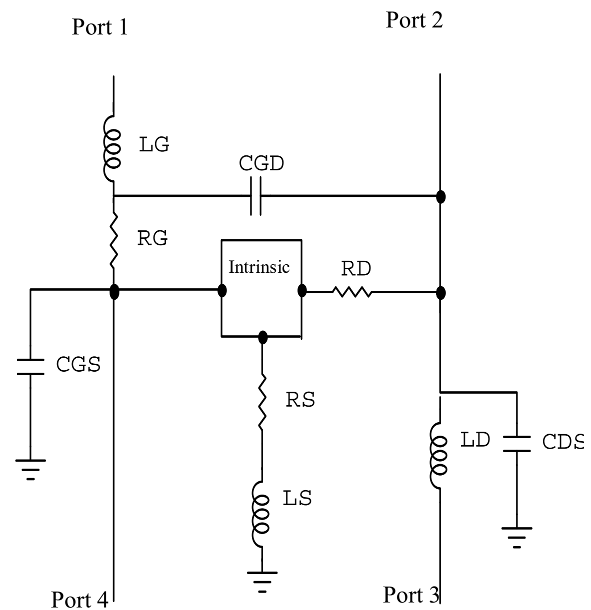

Fig.4. Unit Cell: Square box- intrinsic, four port network- extrinsic parameters

2.2 Device assembly

To assemble the large device we used a simple network. We feed the signal at the gate of first cell and took output at the drain of last as shown in the Fig.5. In the assembling network parameters are mostly dominated by the end values of the transistor metal structure, as in Table.2 gate inductor LGe, drain inductor LDe, gate to drain end capacitor CGDe, drain to source end capacitor CDSe as in Fig.3. We used optimization method in AWR [8] to find the suitable values for this network parameters. The network parameters are given in Table.2. We scaled LS, RS, RD linearly by a factor of 4 as in Table.2 and cascade four UCs to give equivalent to the 2x100um transistor.

Table.2. Parameters of assembling network

Extrinsic of 2x100		Unit Cell			Outer Network	
LS	9.748 pH	Linear	LS	28.94 pH		
RS	1.30 Ohm		RS	5 ohm		
RD	2.005 Ohm		RD	8.3 ohm		
LG	56.026 pH	Optimized	LG	10.02 pH	LGe	36.67 pH
LD	52.288 pH		LD	9.932 pH	LDe	43.9 pH
RG	2.19 Ohm		RG	1.5 ohm		
CGS	26.948 fF		CGS	5.873 fF	CGSe	0 pH
CGD	19.286 fF		CGD	0.682 fF	CGDe	17.77 pH
CDS	4.251 fF		CDS	3.699 fF	CDSe	24.71 pH

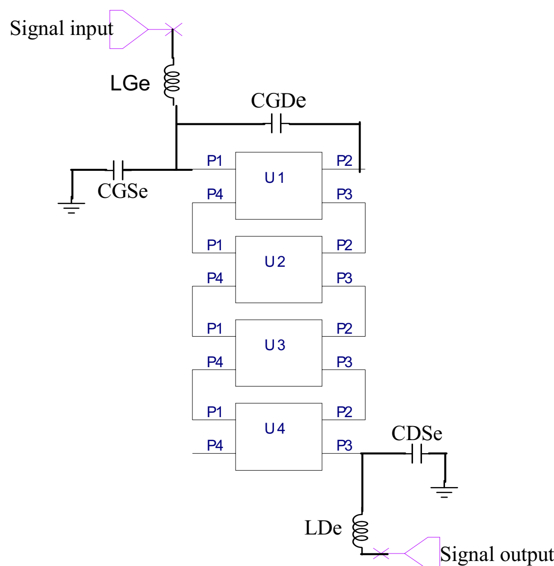

Fig. 5: Interconnection structure of four unit cells with outer network

3 MODEL VERIFICATION

The experiment was based on the TriQuint PHEMTs of 2x100um transistor. The model was verified from 500 MHz to 50 GHz. S-parameter responses show excellent match with the measured data and extracted model. Fig.6 shows the s-parameter curves. The distributed model performs almost the same as the measured data. The gain curve is also excellent shows in the figure.

4 DISCUSSION

Simple linear scaling laws do not allow us to accurately decompose a large device into the combination of several small devices. The outer network gate-drain inductance and gate/drain capacitance we found to be significant proportion of the access network. Although the gate/drain inductors are series connected the total value of inductance seen at gate/drain terminal is reduced. The implication is that for higher frequencies the effectiveness of unit cells is reduced by the distributed nature of the network. The gate-drain capacitance is dominated by the end effect. Drain/source capacitance are not equally distributed and we would like to investigate it later.

This means some end effect work within the transistor metal ends that does not allow distributing a certain part of lumped element values, and force the elements not to scale linearly. To overcome the end effect problem, optimization could be an effective technique to determine the end parameters and produce a good match the scaling device.

5 CONCLUSION

A new lumped element distributed modelling technique of PHEMT has been proposed. The idea of using unit cell as a building block to scale big size transistor, has been proved efficient and by the simulation results. This technique works only by recognizing the distributed nature of all the extrinsic metallization. The model will be used to test the performance in an amplifier circuit in our future work.

Acknowledgments

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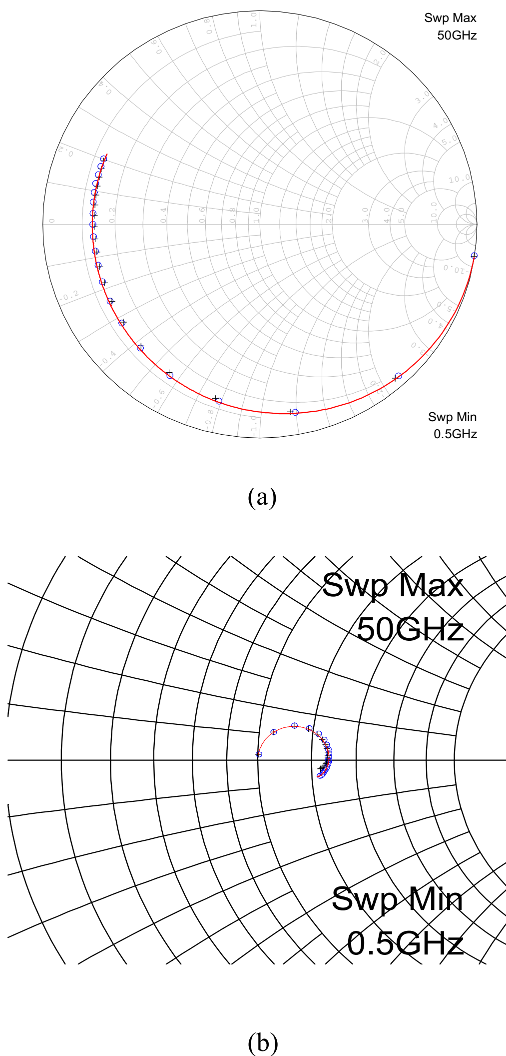
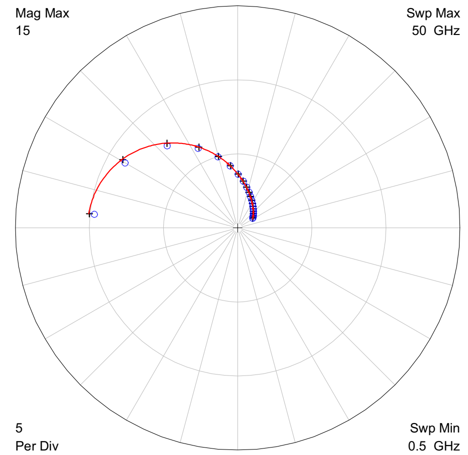
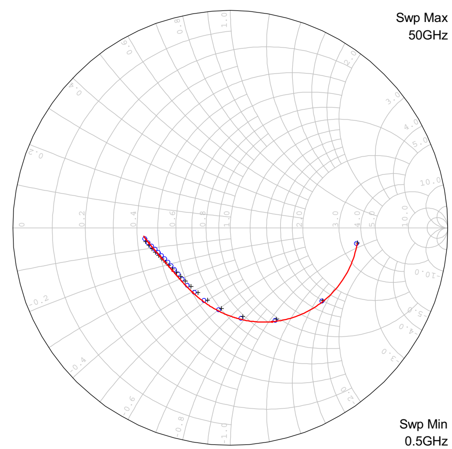


(a)

(b)



(c)



(d)

Fig.6. S-parameter responses: (a) S11, (b) S12, (c) S21, (d) S22. Circle-Measured data, Plus-extracted model, Solid lines- distributed model