Impact of the Semiconductor Diode Structure on the Virtual Local Oscillator Leakage of GaAs Sub-Harmonic Mixers

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***Abstract*— Diode mismatch in an anti-parallel diode mixer results in an unwanted virtual leakage at twice the local oscillator pumping frequency. Random variability in a fabrication process is one of the sources of diode mismatch. In some fabrication processes, a diode usually consists of a transistor with source and drain shorted together. The layout of this structure introduces a systematic source of diode mismatch. An informed selection of the fabrication process is crucial in minimizing the systematic source of diode mismatch and improving the virtual local oscillator leakage.**

***Index Terms*— Mixers, Microwave Mixers, Millimeter wave mixers.**

I. Introduction

Frequency conversion from an intermediate frequency to radio-frequency in a sub-harmonic mixer involves mixing the intermediate frequency with a multiple of the local oscillator (LO) pump frequency. Sub-harmonic mixers that switch at a virtual local oscillator frequency that is twice the pump frequency can be built by connecting two Schottky diodes in an anti-parallel arrangement as shown in Fig 1. Such mixers are referred to as anti-parallel diode (APD) mixers. A pump signal operating at half the virtual LO frequency can overcome the output power limitations of millimeter-wave fundamental oscillators [1], [2].

An ideal APD mixer, one in which the diodes are perfectly matched, does not generate any virtual leakage at the even harmonics of the LO frequency. However, diode mismatch can result in unwanted virtual LO leakage. It can be studied from the asymmetry in the intrinsic diode parameters and the dc offset voltage generated in an APD mixer [2], [3]. Diode mismatch is often introduced by random variations in the fabrication process [4].

Diode mismatch can also arise due to systematic effects. One such effect is due to the presence of inescapable layout asymmetry that is an artifact of diode geometry. This layout asymmetry can lead to a systematic asymmetric self-heating in an APD mixer. The effects of layout asymmetry can be inferred from the statistics of diode mismatch. A correlation between virtual LO leakage and the asymmetry in series resistance has been attributed to the presence of a systematic asymmetric self-heating [5].

A methodology to identify the systematic effects arising in a fabrication process is presented. Identification of the severity of systematic effects can be used to make an informed selection of fabrication processes that would result in improved virtual LO leakage.

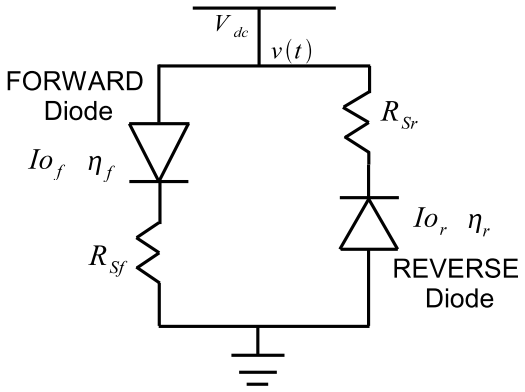

Fig. 1. The figure shows a model of diode asymmetry resulting from diode mismatch in an anti-parallel diode circuit.

DC offset statistics of an APD circuit population can be used to identify the presence of systematic sources of diode mismatch. If a bias exists in the dc offset measured across an APD circuit population, then it points to the presence of a systematic asymmetric self-heating. Two APD circuit populations fabricated using a Gallium Arsenide (GaAs) high-electron mobility transistor (HEMT) process and GaAs hetero-junction bipolar transistor (HBT) process have been used in the investigation.

A clear bias has been found in the dc offset statistics of the HEMT APD circuit population in contrast to a mean-zero dc offset observed in the HBT APD population. This has been used to show that an unavoidable layout asymmetry can result in systematic asymmetric self-heating that leads to a systematic diode mismatch. But if the statistics were to show a mean-zero dc offset, then it points to an absence of systematic effects and diode mismatch is largely a product of random process variation.

The statistics of dc offset and virtual LO leakage have been used to show that the HEMT APD circuits are more susceptible to systematic asymmetric self-heating effects than the HBT APD circuits. Consequently HBT APD circuit have relatively better match and lower virtual LO leakage.

Section II describes the device processes used and the inescapable asymmetry evident in the HEMT APD circuit lay-

out. An analysis showing the link between the bias in dc offset statistics and asymmetric heating is derived in Section III. Section IV and V describe the measurement and the results of dc offset and virtual LO leakage. Finally Section VI discusses various aspects of the results.

II. Mixer Layouts

The characteristics of WIN Semiconductor's GaAs HEMT and GaAs HBT processes utilized in this investigation are shown in Table I. The HEMT's gate-metallization has been

Process	HEMT	HBT
Lithography	E-Beam	Optical
Process f_T	95 GHz	65 GHz
Feature Size	0.15μm	1μm
Junction Area	0.15μm $\times$ 10μm	7μm $\times$ 7μm
Number of Fingers	2	-
Orientation	Planar	Vertical

TABLE I
SEMICONDUCTOR FABRICATION PROCESSES

used to form the Schottky junction and its source and drain metal contacts are combined to form the ohmic contact.

WIN HBT Schottky diode is formed by the junction between the first interconnect metal and the lightly n-doped collector. The ohmic contact is formed by collector metal contacting with the heavily n-doped sub-collector layer [6].

A. Layout Asymmetry & Systematic Asymmetric Self-Heating

An APD circuit using HEMT diodes is shown in Fig 2. The circuit is designed to maximize symmetry. However an inescapable asymmetry is present in the circuit layout. This is in part due to the planar geometry of the two-finger HEMT diode and secondly due to the different metallizations used for the anode and the cathode. The FORWARD diode is characterized by relatively large metal anode connection to the electrical ground and a smaller gate (cathode) contact connected to the 50 Ω transmission line. These connections are reversed for the REVERSE diode.

The layout asymmetry in addition to the planar geometry of the HEMT structure creates a situation where by one diode dissipates heat more effectively than the other. Although it could be speculated as to which diode disposes heat less effectively, the situation is also complicated by the heat flow through the substrate.

APD circuits using HBT diodes are shown in Fig 3. They offer more immunity from the systematic asymmetric self-heating. Although a degree of asymmetry is present in the HBT APD layout in Fig 3, its effects are tempered by the vertical geometry of the HBT diodes. A significant proportion of the heat generated in a diode flows in the vertical direction to the substrate. A smaller proportion nonetheless is present in the planar direction but its effect is minimal. The thermal resistances of the HBT diodes may not be identical, but the vertical flow of heat makes a HBT APD circuit less susceptible to the systematic asymmetric self-heating.

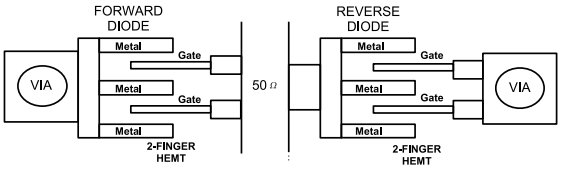

Fig. 2. A simplified layout of a HEMT APD circuit (not drawn to scale) is shown. In the diode labeled FORWARD, the metal is connected to ground, where as the gate is connected to the 50 transmission line. These connections are reversed for the diode labeled REVERSE. This results in a layout asymmetry.

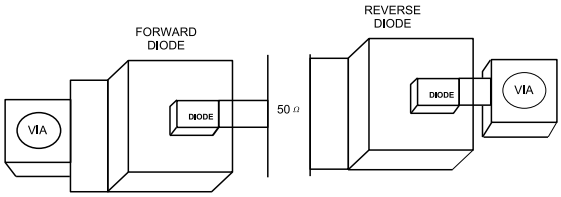

Fig. 3. A simplified layout of an HBT APD circuit (not drawn to scale) is shown. The vertical geometry ensures that significant proportion of heat being dissipated flows to ground. The proportion of heat dissipation in the planar direction is substantially lower.

III. Quantitative Measure of Asymmetric Heating

This section uncovers the relationship that exists between dc offset and asymmetric heating in an APD circuit with diode mismatch. The current-voltage characteristic of such an APD circuit can be represented by:

$$I(V) = I_{of} e^{\frac{qV}{\eta_f k T_f}} - I_{or} e^{-\frac{qV}{\eta_r k T_r}}, \tag{1}$$

where V is the applied bias, I_{of}, I_{or} are the forward and reverse diode saturation currents and η_f, η_f are the forward and reverse ideality factors (Refer to Fig 1) and T_f, T_r are the forward and reverse junction temperatures and q, k are electron charge and Boltzmann constant respectively.

The saturation currents I_{of} and I_{or} are given by:

$$I_{of} = A^* {T_f}^2 W_f e^{-\frac{q\phi_b}{kT_f}},\ I_{or} = A^* {T_r}^2 W_r e^{-\frac{q\phi_b}{kT_r}}, \tag{2}$$

where A^* is the Richardson constant, W_f, W_r are the forward and reverse junction areas and ϕ_b is the built-in voltage assumed to be the same for both diodes.

Substituting (2) in to (1) and making a few idealizations such as $\eta_f = \eta_r = \eta$ and $W_f = W_r = W$ results in:

$$I(V) = A^* W \left[{T_f}^2 e^{\frac{qV_b}{kT_f}} - {T_r}^2 e^{-\frac{qV_b}{kT_r}} \right], \tag{3}$$

where η , W are the ideality factor and the junction area for both forward and reverse diodes and $V_b = \frac{V}{\eta} - \phi_b$.

The Taylor series expansion of the virtual LO leakage current due to diode mismatch can be written as:

$$I_{2LO}(v) = \sum_{m=1}^{n} \frac{1}{2m!} \left[g_{2m}(V_b)_{|_{V_b=0}} \right] v^{2m}, \tag{4}$$

where I_{2LO} is the virtual LO leakage current, v is the time-varying voltage, V_b is the net dc bias across the junction

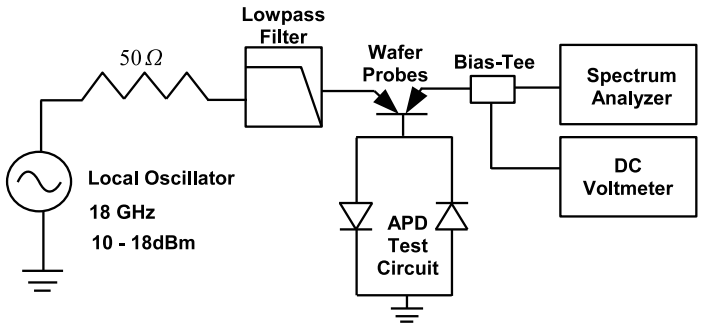

Fig. 4. The setup for measuring dc offset and virtual LO leakage in an APD circuit. The low-pass filter in the setup was used to minimize any second-harmonic leakage coming from the signal generator.

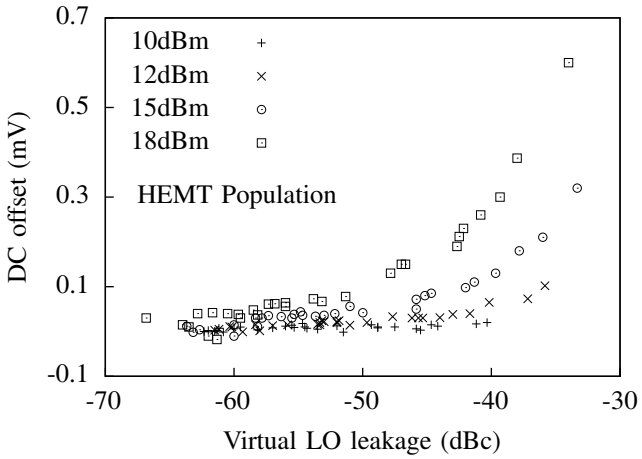

Fig. 5. There is a clear bias in the statistics of dc offset in the HEMT APD population. This bias also increases with the LO drive power. It strongly supports the argument that layout asymmetry is responsible for a systematic asymmetric self-heating.

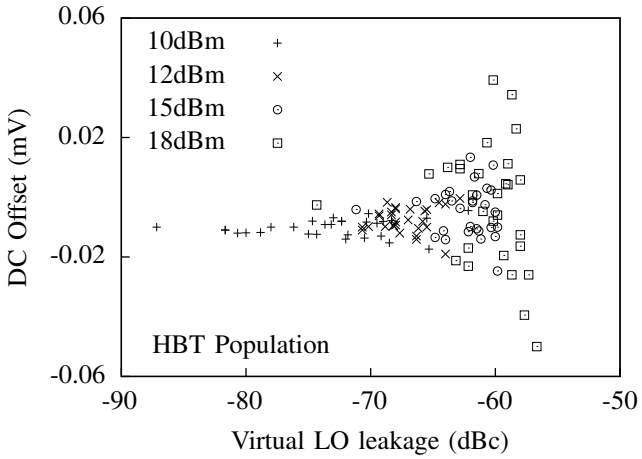

Fig. 6. DC-offset measured across the HBT APD population has a mean of zero. This distribution of dc offset indicates that HBT APD circuits are less affected by systematic effects.

defined in (3) m, n are integers and g_{2m} is the $2m^{th}$-derivative of (1).

The dc-term which is also the first term of the Taylor series in (4), is given by:

$$I_{dc} = \left[g_0(V_b)_{|_{V_b=0}}\right] v^0, \tag{5}$$

where I_{dc} is the net dc current flowing through the APD circuit (excited by the time-varying voltage v) and g_0 is the dc-conductance term given by:

$$g_0(V_b)_{|_{V_b=0}} = A^* W \left[{T_f}^2 - {T_r}^2\right]. \tag{6}$$

The dc offset V_{dc} generated due to mismatch is given by:

$$V_{dc} = I_{dc} \times R = A^* W \left[{T_f}^2 - {T_r}^2\right] \times R, \tag{7}$$

where R is the dc resistance in the APD circuit.

$$V_{dc}\ \alpha \left[{T_f}^2 - {T_r}^2\right] \tag{8}$$

If the forward and reverse diode temperatures T_f and T_r are equal, then the resulting dc offset, given by (8) would always be zero. When T_f and T_r are unequal with some distribution over a population, then the resulting dc offset would have a zero mean.

Alternatively if there were to be systematic effects such as systematic asymmetric self-heating, then a particular diode always has a junction temperature that is greater than the second diode. This shows as clear bias in the statistics of dc offset measured across a population of APD circuits.

IV. Measurement

DC offset and virtual LO leakage of a 28-sample HEMT population and a 29-sample HBT APD population have been measured to identify the presence of systematic sources of diode mismatch.

The test-setup shown in Fig 4 was excited by a single-tone signal with a frequency of 18 GHz. The resulting virtual LO leakage at 36 GHz and the accompanying dc offset were measured for various signal powers of 10, 12, 15 and 18 dBm respectively. The dc offset voltage was measured using a precision voltmeter de-coupled from the spectrum analyzer used to measure the virtual LO leakage by means of a bias-tee. A low pass filter with a stopband attenuation of 50 dB was utilized between the signal generator and the APD circuit input to minimize the second-harmonic of the generator from compromising the integrity of the virtual LO leakage measured at 36 GHz.

V. Results

DC offset statistics of the HEMT APD population shows a clear bias. This can be seen in Fig 5 where the dc offset voltage is plotted against the virtual LO leakage. It is consistent with the implications of (8) that any systematic asymmetric self-heating will result in a bias in the dc offset data. Furthermore this bias also increases with LO drive power, which is a manifestation of greater systematic asymmetric self-heating brought on by the increase in dissipated power.

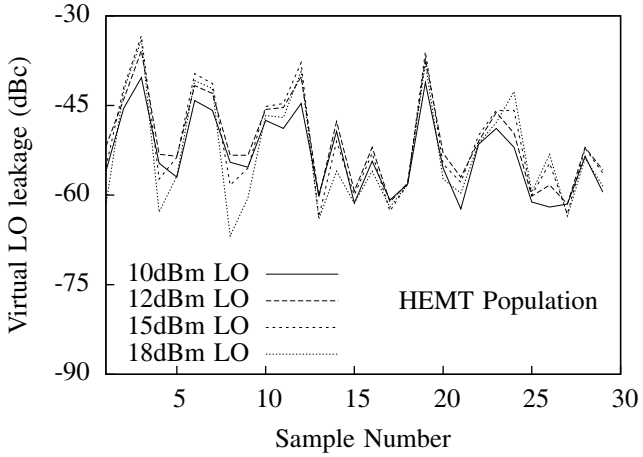

Fig. 7. The HEMT APD population has a significantly higher virtual LO leakage compared to HBT population shown in adjacent figure. This is due to the presence of systematic sources of diode mismatch on top of the random process variation.

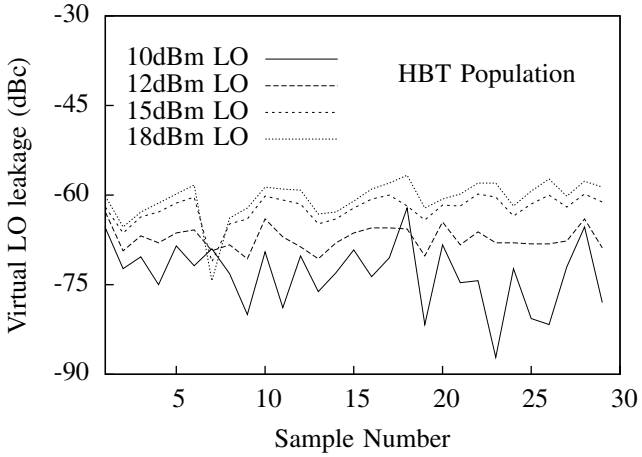

Fig. 8. The HBT APD population has a considerably lower virtual LO leakage than the HEMT population in adjacent figure. This is due to the absence of systematic source of diode mismatch as evident from the mean-zero behavior of dc offset data.

DC offset voltage measured in the HBT APD population follows a random pattern. It is plotted against the virtual LO leakage measured at various drive powers in Fig 6. The dc offset has a mean about zero in stark contrast to the HEMT population. It suggests that the HBT APD structure offers immunity from diode mismatch inducing systematic asymmetric self-heating.

The measured virtual LO leakage of the HEMT APD circuit population is shown in Fig 7. The virtual LO leakage varies approximately between -40 dBc and -60 dBc across the population, for the LO drive power range of 10 to 18 dBm. The HBT APD circuit population in Fig 8 varies between -60 dBc and -80 dBc for the same range of LO drive powers.

The virtual LO leakage in the HBT APD circuit population shows an improvement of at least 15 dB compared to the HEMT APD population. These results demonstrate that a clear bias in the statistics of dc offset correlates with the increased virtual LO leakage observed in HEMT population.

VI. Discussion

It should be noted that the HEMT and HBT processes also differ in terms of diode size. The HBT diode area is larger than the HEMT diode area by a factor of 15. The smaller HEMT diodes are more susceptible to process tolerances than the larger HBT diodes. In addition HEMT APD circuits also suffer from asymmetric heating. These factors work together to cause a substantial increase in dc offset and virtual LO leakage. However the bias in the measured dc offset voltage across the HEMT population in combination with a substantial increase in dc offset voltage with LO drive power strongly indicate that a systematic asymmetric self-heating is the dominant factor responsible for the noticeable increase in the virtual LO leakage.

It is also notable in Fig 8 that a few circuits in the HBT population exhibit similar virtual LO leakage levels even though they have different dc offset voltages. This is contrary to the assertion that dc offset voltage correlates with the virtual LO leakage. This anomaly could be caused by many factors not considered in the analysis such as the difference in the built-in voltages of the diodes. Asymmetry in the built-in voltage of the diodes can also contribute to the dc offset but may not necessarily correlate with the virtual LO leakage.

VII. Conclusion

DC offset in HBT APD circuit population has less systematic bias and this correlates with the improved virtual LO leakage measured. APD circuits using HBT diodes offer superior virtual LO leakage performance over APD circuits using HEMT diodes. The impact of the diode size on the dc offset and mismatch is a subject of an ongoing investigation.

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