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ORIGINAL RESEARCH

Design of a stagger-tuned high-power low-stress capacitive wireless power transfer system

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Abstract

Capacitive power transfer (CPT) has emerged as a promising alternative to traditional inductive methods. CPT offers advantages like cost-effectiveness, reduced weight and volume, and greater tolerance to alignment errors. However, the high-Q resonant circuits used as matching networks can be susceptible to high voltage stress, especially when transmitting substantial power. Consequently, designing matching networks for CPT systems necessitates consideration of multiple parameters, including practical constraints such as component losses and breakdown thresholds. In this work an innovative algorithm is presented for designing practical matching networks in CPT systems. The algorithm conducts a methodical search of potential solutions, and converges on component values that maximize power transfer efficiency whilst also minimizing component voltage stress. The proposed algorithm is demonstrated theoretically and experimentally.

1 | INTRODUCTION

Wireless power transfer (WPT) is capable of providing efficient, safe, and sustainable ways of powering various heavy and industrial transport vehicles such as electrified railway vehicles (ERV) [1, 2]. WPT systems based on near-field coupling may be classified as i) inductive power transfer (IPT) and/or ii) capacitive power transfer (CPT). Traditionally, IPT has been preferred for medium power and medium distance WPT applications such as electric vehicle (EV) chargers and wireless ERVs. However, CPT technology has a number of potential advantages, including; lower cost and lighter weight due to simple construction (plane metallic coupler plates), less sensitivity to nearby objects [3], and better robustness against misalignment between primary and secondary elements [4].

In a typical CPT system with simple primary and secondary L-C matching networks, shown in Figure 1, the real and reactive power flow through the coupling capacitance are given by (1) and (2), respectively [5].

$$P_{coupler} = \omega C_m V_{p1} V_{p2} * \sin(\theta), \quad (1)$$

$$Q_{coupler} = \omega C_m V_{p1} V_{p2} * \cos(\theta). \quad (2)$$

Maximizing the power transferred through the CPT system may be achieved by maximizing the terms on the right-hand-side of (1), within practical limits. For example, increasing the operating frequency $\omega(= 2\pi f)$ is effective, but is limited in practice by the capabilities and cost of high-speed power switching devices. Increasing the coupling or mutual capacitance (C_m) will also increase the transferred power, but is limited by the dimensions and materials used in the coupler, and the need to avoid dielectric breakdown. It has also been shown that to maximize the power transfer through the coupling capacitor whilst minimizing the voltage across it, the phase shift (θ) between V_{p1} and V_{p2} should be 90° [5]. As the magnitude of the coupling capacitance and operating frequency are limited in practice, most high-power CPT systems exhibit very large voltages in the primary matching network and across the coupling plates (V_{p1} and V_{p2}). These high voltages are often in the kV range and hence can result in dielectric breakdown and safety concerns. Consequently, minimization of the latter voltages is important in designing any high-power CPT system.

Based on the above design criteria, a high-power and highly efficient CPT system with minimized voltage stress requires: (i) minimum reactive power in the matching circuit (unity power factor at the output of the inverter), (ii) a large

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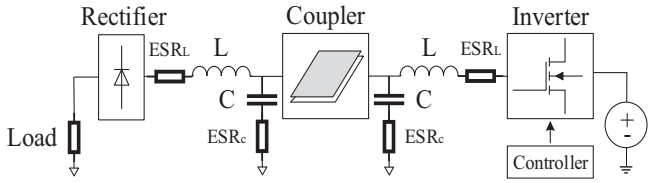

FIGURE 1 CPT typical system structure.

coupling capacitance, and (iii) 90° phase shift between the primary and secondary coupler voltages. These design criteria have been encountered in various CPT development projects. First, an analytical approach to voltage stress minimization is outlined in [6]. This work, however, does not practically demonstrate the reduction in voltage stress afforded by the proposed algorithm and does not attempt to enforce a 90° phase shift. Simple and low cost CPT systems with LC matching networks were proposed in [7, 8], however the topology suffered from high voltage stress on the coupler, largely as a result of the small phase-shift (5°). A double-sided LCLC-matching circuit that could achieve a maximum of 54° phase shift across the coupler was reported in [9]. In [10], an LCL-LC design was reported that achieved 55° phase shift. In [11], the circuit topology of CLL-LC achieved 58° phase shift between the couplers' voltages. In [12], an LC-CLC design achieved a phase shift of 42°. In [13], a double-sided two coils-compensated topology could achieve 68° phase shift. In [14], LCL-CL topology demonstrated accommodating of 47° phase shift between the voltages on either side of the coupling capacitor.

None of the latter topologies achieved a 90° phase shift in voltage across the coupler. Moreover, because of being limited in coupling capacitance, none of these systems could achieve beyond 2.1 kW of power transfer. This is because the systems shown have not adhered to the three design requirements for a high-power application. In addition, these systems were designed for ideal conditions, where losses in the passive components were neglected. In a recent study, a loosely-coupled CPT system using an LC-CLC circuit, was optimally designed and could achieve 90° phase shift [9]. Whilst this system reduced the voltage stress on the coupler, adding an extra capacitor to the secondary side increases the matching network complexity. Moreover, this CPT system was designed and validated for low power applications (2kW) under ideal conditions. Since high power throughput incurs high heat losses in passive elements, employing a simple matching network (LC-LC) is desirable. Achieving requirements for maximum power transfer has yet to be shown possible with this simple network.

In this article, we present an innovative staggered numerical design approach, specifically tailored for the design of practical matching networks in high-power CPT systems. The proposed approach aims to alleviate voltage stress in these systems while simultaneously ensuring high power, efficiency, and simplicity of the matching network. The two key contributions of our proposed approach can be summarized as follows:

- Enabling efficient transmission of high power (~100 kW), and applicable to effectively accommodate both large and small coupling capacitances, making it versatile for a wide range of applications.
- A distinctive aspect of our approach is the regulation of a precise 90° phase shift between the voltages of the coupler. This plays a pivotal role in realizing a significant reduction in voltage stress, contributing to the overall robustness and reliability of the CPT system.

Furthermore, the proposed design approach considers equivalent series resistance (ESR) of standard components during the design process. This ensures that our design and model are high-fidelity and practical, making them suitable for large-scale CPT implementations.

In the following sections the proposed approach is presented, and its effectiveness is validated through modeling for a real high-power ERV application which is shown to be capable of 100 kW power transfer per set of coupling plates and matching network. The same approach is then used to design and build a scaled-down prototype. The experimental results closely align with simulation findings, affirming the high fidelity and reliability of the design approach.

2 | PROPOSED DESIGN ALGORITHM

The proposed design algorithm outlines a systematic approach to designing and optimizing a matching network for double-sided LC-CPT system, as shown in Figure 1, considering various parameters, component availability, and the need for iterative tuning to meet specific performance criteria. The proposed algorithm, shown in Figure 2, is a structured process to ensure the coupler functions as intended in wireless power transfer applications.

It begins with the development of the initial concept for the coupler and then progresses to modeling the coupler using software like ANSYS Maxwell or mathematical calculations. Key parameters such as mutual capacitance (C_m), the matching network component values including L_1, L_2, C_{ex1}, C_{ex2}, and their ESRs are calculated and selected with consideration for market availability. The flowchart then guides the designer through iterative steps to fine-tune the design, ensuring that the desired resonance frequency, power transfer efficiency, a 90° phase shift and unity power factory at the primary side are achieved. Once these criteria are met, the design process is considered complete. However, if the desired performance is not attained, the flowchart provides instructions for adjusting inductors and capacitors, recalculating their ESR, and returning to specific steps to optimize the design.

The latter novel and systematic design method ensures that the CPT coupler functions efficiently and effectively in wireless power transfer applications. After initialization of a CPT model using the calculated C_m and selected initial values for external capacitors and inductors and their calculated ESRs, two main conditions of desired power and efficiency and 90° phase shift are checked separately. Power and efficiency are maximized via a matching network within the stagger-tuned system. To do so, C_{ex1} is increased in iterative steps. L_1 is recalculated to

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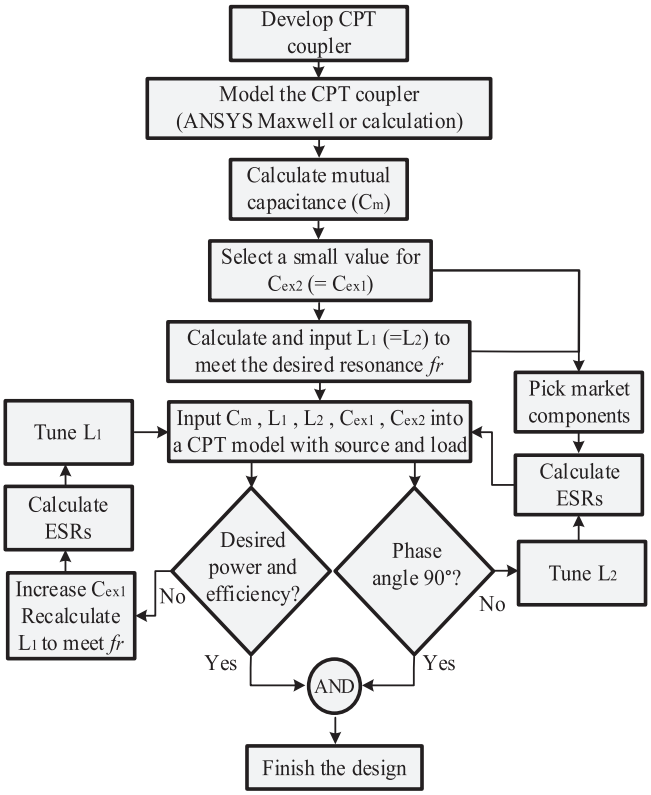

FIGURE 2 Proposed design algorithm for a CPT system.

meet the targeted resonant frequency at each iteration as well as ESRs for both C_{ex1} and L_1. Then by further tuning of L_1, the desired power and efficiency will be reached for a given load. This approach (increasing the size of L_1 in subsequent to increasing C_{ex1}) increases voltage gain by making the size of L_2 greater than the size of L_1, meeting the condition for large plate voltages according to (1) [5]. This process, however, potentially increases voltage stress on couplers, which is accounted for in the proposed algorithm through phase shift regulation. To do so, 90° phase shift in coupler's voltages is accomplished through the tuning of L_2 slightly away from exact resonance. This process will not only reduce voltage stress under a constraint of power delivery, but, also leads to having close-to unity power factor at the primary matching circuit leading to minimized reactive power losses for a given load, as given by the power Equations in (1) and (2) [5].

The details of the proposed design approach and its working principles will be further explored in the following section which presents the design of a CPT system for an ERV.

3 | PROPOSED DESIGN FOR ELECTRIFIED RAILWAY VEHICLE

3.1 | ERV system requirements

The design of a CPT system is conducted to meet the 100 kW power requirement (per carriage) of a common ERV [13, 15].

TABLE 1 Specifications of ERV [15].

Parameter	Value	Unit
Length (Bogey)	7	Meters
Width	2.65	Meters
Track Gauge	1.40	Meters
Number of Bogeys	5	N/A
Access height	326	Millimeters
Power supply voltage	750	V_{dc}
Power requirement	500	kW
Power requirement (per carriage)	100	kW

The specifications of this are summarized in Table 1, taken from [15]. The CPT system (i.e. the coupler plus matching circuits) is designed to satisfy the latter specifications. The sizing of the plates is fit to comply with the available space of the bogey.

The power requirement will inform a key design parameter of the system, alongside designing for high efficiency and lower voltage stress. An operational voltage of $750V_{dc}$ is to be adopted for this investigation in accordance with common railway electrification standards [15].

3.2 | Coupling plate design

The CPT coupler and plates were selected to fit within the underside of the ERV bogey [15]. Since the proposed rectangular coupling is a two-plate design, where the return path is satisfied by a ground connection, the calculation of all capacitances in the environment is much simpler due to the lack of parasitic capacitances between coupling surfaces. However, there still exists leakage capacitances to the wheels, as well as to the chassis and road. In order to find an estimation for coupling capacitance, the simplified 4 plate model from [16, 17], was adopted that reflects the general charging environment. This was then modelled in ANSYS Maxwell using finite element analysis to determine a coupling capacitance between the primary plates, whilst taking into consideration these leakage capacitances. Using this simplified model, the upper and lower bounds of where the coupling capacitance may lie is determined. A maximum airgap case of 300 mm and a smaller airgap of 100 mm are selected. Using this model, the relative coupling capacitances are calculated to be 100.17 pF (large airgap) and 206.15 pF (small airgap). Table 2 summarizes the two proposed scenarios and Figure 3 shows the simplified charging environment model.

3.3 | Analysis and selection of passive components

To correctly design and model the CPT system to be applicable in the real world, critical system parameters associated with system losses are not neglected and the market availability for the component selection is investigated. In designing the

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TABLE 2 Physical design of CPT coupler.

Design parameter	Design value
Plate length	3.65 m
Plate width	1.30 m
Total plate area	4.745 m^2
Thickness	5.0 mm
Material	Aluminum
Plates per coupling (per bogey)	2
Airgap (Z)	100 mm/300 mm

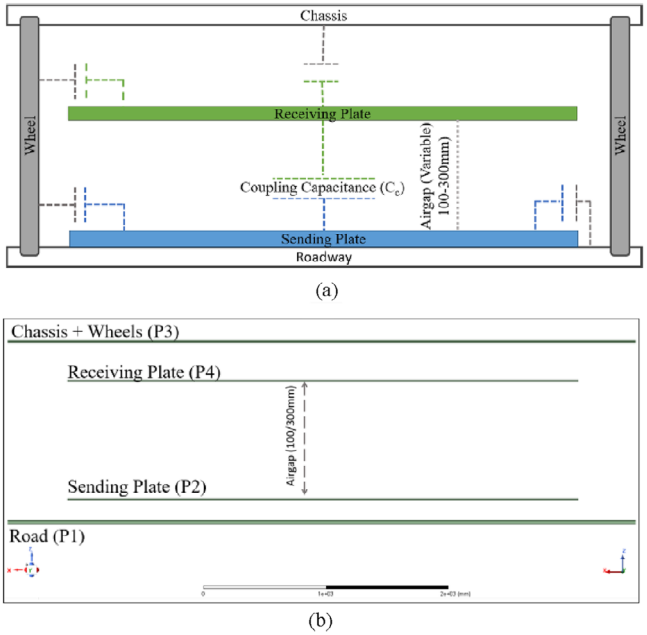

FIGURE 3 (a) CPT charging environemnt. (b) ANSYS simplified model.

double-sided LC matching topology selected in this article, the parasitic/series resistances of the passive components are determined through assessment of commercially available parts that meet the requirements of this CPT system and calculated based on market data.

The real power dissipated in the passive components is a result of the size of the ESR, and therefore the component Q. To ensure high efficiency in a CPT system with double sided LC matching, reduction of losses in the primary matching network is critical [5]. High efficiency can be observed when the losses in L_1 are minimized through reduction of physical winding size. This can be achieved through designing C_{ex1}, such that the inductor reduces in size to meet the resonant frequency of the system [18]. Firstly, as demonstrated by (3), by increasing the value of the matching capacitor, and assuming a constant dissipation factor (which is commonly a function of frequency) [18], capacitor's losses are decreased as the parasitic component is reduced. This allows the reduction in size of resonant inductor without incurring additional loss.

$$DF = \frac{ESR}{Xc} = \frac{ESR}{\frac{1}{j\omega C}}. \tag{3}$$

The capacitors are modelled on Vishay Specialist Ceramics, with a 10–15 kV_{ac} limit. These are selected to minimize ESR, as this component is available in variety of capacitance values with a fixed dissipation factor. The dissipation factor is thus kept below 0.07% [19]. The resistance of the inductors is calculated following the design guidelines found in [20]. Due to the variation of the capacitance, the size of the inductor changes to meet resonance. This means series resistance of the inductor also changes at each incrementation stage. The inductors are modelled from 48AWG Litz Wire with 370 strands, giving an overall current carrying capacity of 300 A (~11.1 mm diameter cable), suitable for this high-power application. The equations for calculating the AC resistance of the matching coils is shown in (4) [21].

$$\frac{R_{AC}}{R_{DC}} = H + \left[K + u\left(\frac{D_o}{c}\right)^2\right]\left(\frac{D_i}{D_o}\right)^2 N_s{}^2 G, \tag{4}$$

where H is resistance ratio of individual strands of wire, N is number of strands, D_i is diameter of individual strands, D_o is diameter of overall cable, G is Eddy-current bias factor, K and u are constants based on inductor construction, and c is determined from spacing of inductor turns from winding diameter [21]. R_{DC} refers to the maximum DC resistance of a given cable per 1000 feet (~304 m), and is given by (5) [22]

$$R_{DC} = \frac{Rs\left(1 + \sum_{i=1}^{N_B} 0.02\right)(1.03)}{N_S}, \tag{5}$$

where R_s is maximum DC resistance for strand diameter from [21] and N_B is bunching operations in construction, assumed to be 1. This gives $R_{DC} = 0.067\ \Omega/m$. Then, the ESR of the total winding is given by

$$R_{ESRL} = \left(\sqrt{\frac{L(l)}{\mu_r \mu_0 \pi r}}\right)(2\pi r)(R_{AC}), \tag{6}$$

where L is inductance, l is inductor length, μ_r is permeability constant, μ_0 is permeability of air, and r is radius. To find the equivalent AC resistance for the given inductor construction, it is taken that K = 2, with H = 1.2, G = 0.31, u = 3.29 and c = 2.5 [21]. Now, from (4), an AC/DC ratio of 1.019 is calculated, giving AC resistance $R_{AC} = 0.069\ \Omega/m$. This value is then used when calculating the required length of each inductor given in (6). Table 3 summarizes the systems parameters for use in the simulation environment.

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TABLE 3 Systems parameters for use in the simulation.

Parameter	Value
Inverter resistance	140 mΩ
Diode forward voltage	0.71 V
Smoothing capacitor	1 nF
Switching frequency	2 MHz
Dissipation factor of $C_{ex1,2}$	0.07%
Resistance of inductor	0.069 Ω/m
Input voltage	750 V
Load	50 Ω

4 | DESIGN OF MATCHING NETWORK FOR ERV

Now, with the CPT system outlined and passive component parameters identified, the design algorithm outlined in Section 2 is executed for both high and low coupling models. To avoid repetition, the design details in this section are only presented for the high coupling model (206.15 pF coupling capacitance).

4.1 | Stagger-tuned LC system design analysis

C_{ex2} was kept at 300 pF while varying C_{ex1} from 100 pF to 2500 pF. Then L_1 was adjusted to achieve a resonance frequency of 2 MHz at each iteration. Figure 4a demonstrates that power transfer exceeding 100 kW was achieved with C_{ex1} values ranging from 1000 pF to 2500 pF, meeting the design requirement. However, in Figure 4b, it is evident that achieving this power level results in high voltage profiles, with substantial voltage stresses on external capacitors and plates (15–25 kV). This elevated voltage is primarily due to the phase angle (15° to 20°) between the couplers' voltages.

4.2 | Inductor tuning in the stagger tuned LC circuit

Now, L_1 and L_2 are shifted away from ideal resonance to meet high power requirement while limiting voltage stress on couplers. Correct tuning of this system will exhibit both (i) a 90° phase shift in couplers' voltages and (ii) unity power factor at the input (inverter soft-switching) [5]. This was achieved through conducting an optimal power transfer research as proposed by [23], whereby the system is tuned such that the above criteria are observed. From the findings in Figure 5a, as L_1 was tuned, 144 kW of power was achieved, exceeding the minimum requirement for ERV, at 89% efficiency. As also shown in Figure 5b, by tuning L_2, phase shift between couplers' voltages is regulated to 90°, which keeps the plates voltages at a maximum of 8kVrms (at 90°). This was obtained at C_{ex1} of 2500 pF and C_{ex2} of 300 pF. Table 4 summarizes the designed parameters.

TABLE 4 Designed parameters for matching circuit.

System design parameter	Value
High coupling capacitance system	
Primary external capacitor	2500 pF
Secondary external capacitor	300 pF
Tuning inductor	2.37 uH and 11.2 uH
System resonance frequency	2 MHz
Plate structure	2 Plate (Rectangular)
Low coupling capacitance system	
Primary external capacitor	1500 pF
Secondary external capacitor	300 pF
Tuning inductor	4 uH and 14.7 uH
System resonance frequency	2 MHz
Plate structure	2 Plate (Rectangular)

TABLE 5 Performance of the proposed system.

Performance metric	Value
High coupling capacitance system	
Power transfer to load	144.20 kW
Efficiency	89.63%
Primary voltage (V_{P1})	7.01 kVrms
Secondary voltage (V_{P2})	8.03 kVrms
Plate voltage phase angle (θ)	90° ($1.2500e^{-7}$s)
Low coupling capacitance system	
Power transfer to load	122.89 kW
Efficiency	88.77%
Primary voltage (V_{P1})	10.1 kVrms
Secondary voltage (V_{P2})	9.7 kVrms
Plate voltage phase angle (θ)	90.1° ($1.2507e^{-7}$s)

4.3 | Simulation results from the designed system

The designed system was analyzed through assessment of power transfer, voltage stress, efficiency, and phase angle in coupler voltages and at the input. Table 5 shows the results of the simulation, which are very close to the designed values, for both high-coupling capacitance and low-coupling capacitance systems. The close-to-90° phase angle informs the achievement of voltage stress minimization. In addition, efficiency of both systems exceeds 88% when at least 120 kW of power is being transferred.

Figures 6 and 7 show the coupler voltages and input voltage and current waveforms for both high and low coupling capacitance systems. Both a 90° phase shift between the voltages, and close-to-unity input power factor was observed at whilst maintaining a sub-11 kV RMS voltage for V_{p1} and V_{p2}. Table 6 compares performance of the proposed method with some previously proposed CPT topologies in

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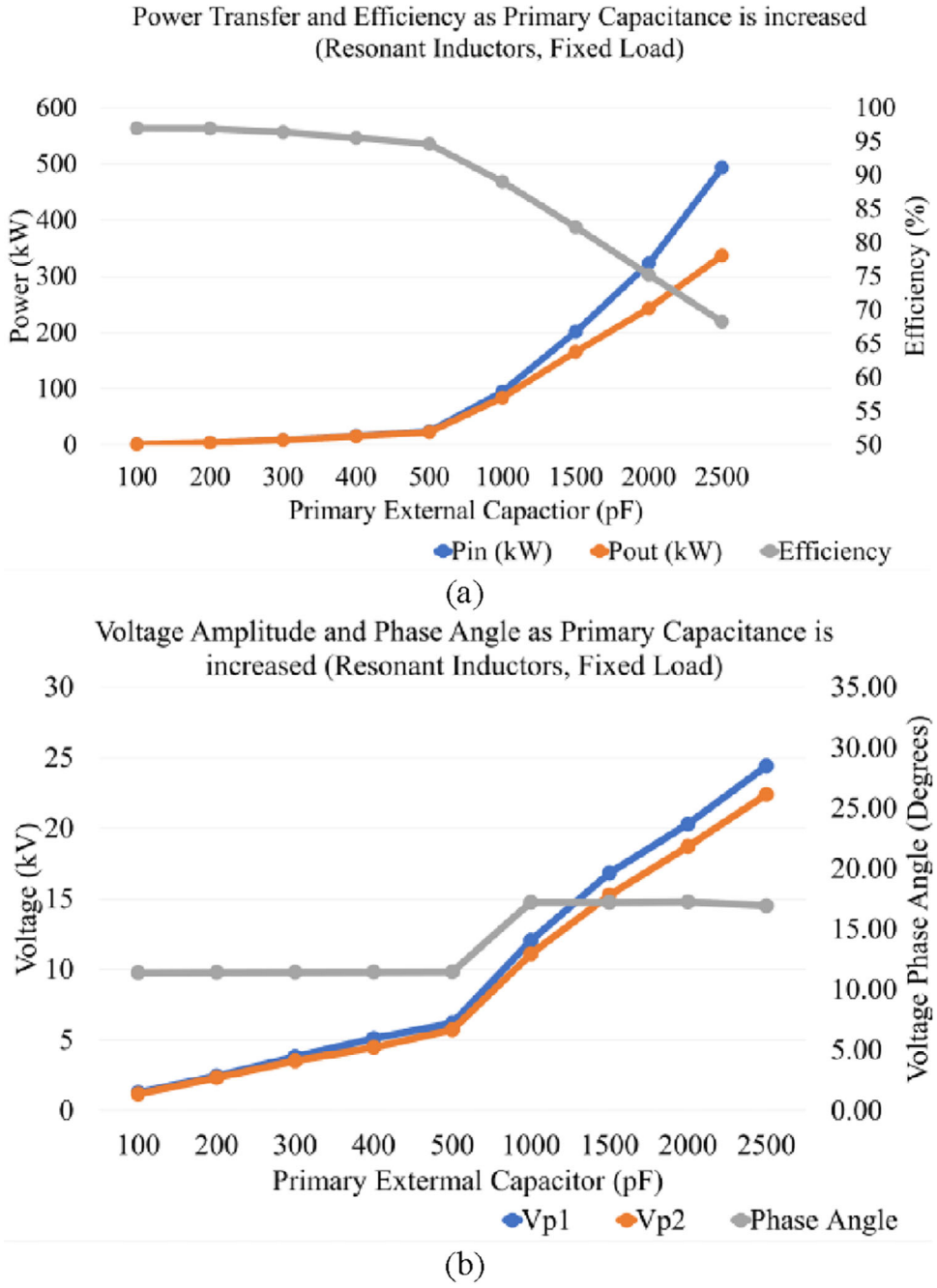

FIGURE 4 (a) Power transfer and efficiency as C_{ex1} is increased. (b) Voltage amplitude and phase angle as as C_{ex1} is increased.

TABLE 6 Performance of the proposed system compared with existing CPT systems.

Reference	Power	Vin	Frequency	V1 (RMS)	V2 (RMS)	Angle	Airgap
LC-LC (proposed)	144 kW	750 V	2.0 MHz	7.0 kV	8.03 kV	90°	100 mm
LC-LC (proposed)	122 kW	750 V	2.0 MHz	10.1 kV	9.7 kV	90.1°	300 mm
LC-CLC [9]	2 kW	300 V	0.8 MHz	5.36 kV	5.36 kV	90°	150 mm
LCLC-LCLC [4, 9]	2.4 kW	265 V	1.0 MHz	5.09 kV	5.09 kV	54°	150 mm
LCL-LC [9, 10]	1.8 kW	270 V	1.0 MHz	5.12 kV	5.08 kV	55°	150 mm
LC-CLC [9, 12]	1 kW	200 V	0.6 MHz	4.2 kV	5.99 kV	42°	150 mm
EFR approach [9, 13]	700 W	350 V	2.0 MHz	1.47 kV	1.74 kV	68.4°	17 mm

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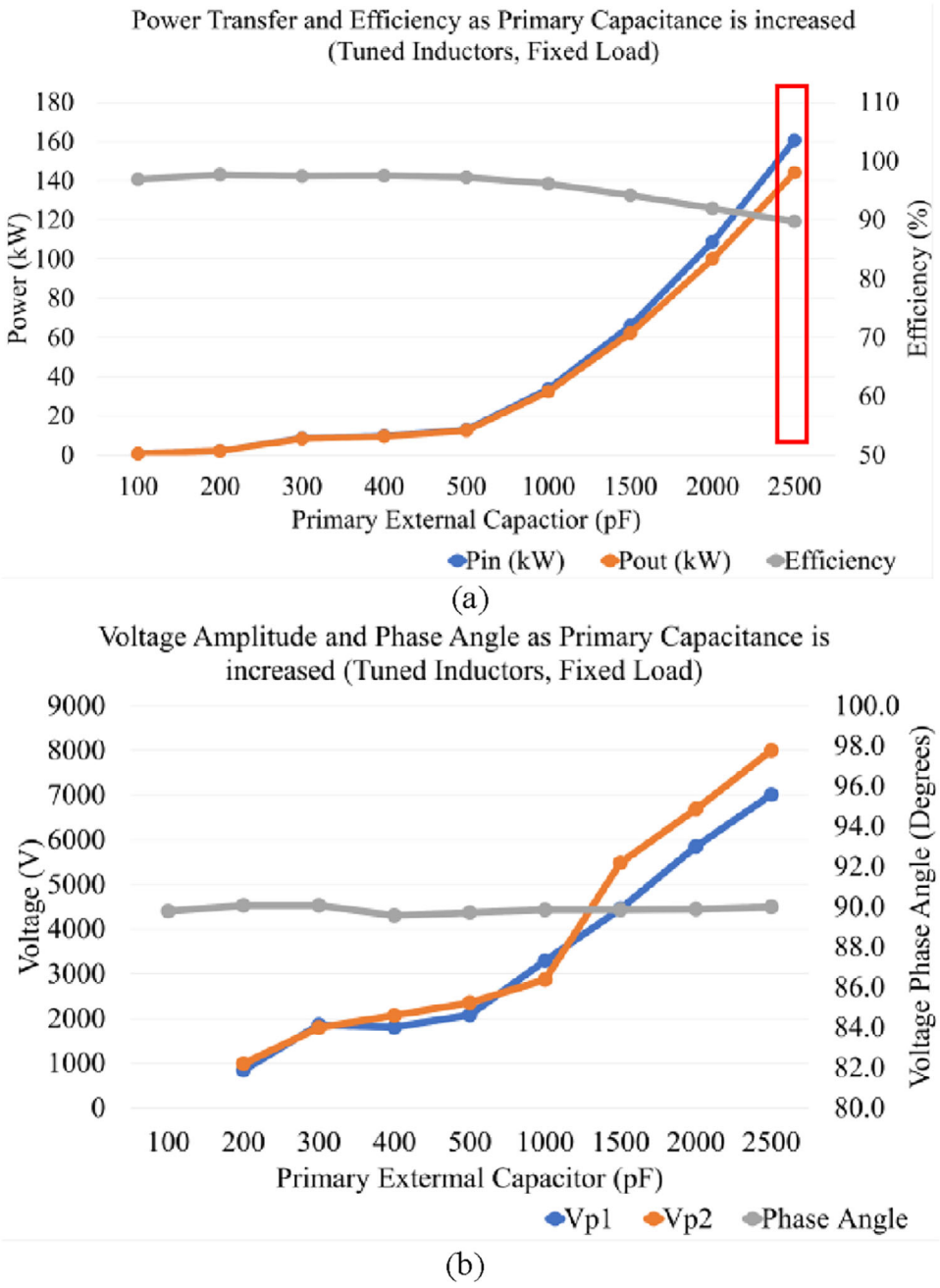

FIGURE 5 (a) Efficiency and power transfer as C_{ex1} is increased and inductors are tuned. (b) Voltage amplitude and phase angle as C_{ex1} is increased, and inductors are tuned.

terms of power transfer capability, primary and secondary voltage stress, phase angle and airgap size. Both small and large coupling capacitance systems exhibit high power transfer capability, relatively low plate voltages due to voltage phase difference of close to 90°. It should be noted that the performance results of the proposed method are simulation based. Therefore, to experimentally validate these results, a downscaled prototype version of the designed CPT system using the proposed method will be presented in the following section.

5 | DOWNSCALED CPT SYSTEM DESIGN

A downscale laboratory prototype is implemented by employing the same design method proposed in Section 2. The goal is to validate that the design process results in a system that exhibits the 90° phase shift between the voltages and close-to-unity power factor at the input. The two-plate structure is similarly investigated in a rectangular format with the details tabulated in Table 7.

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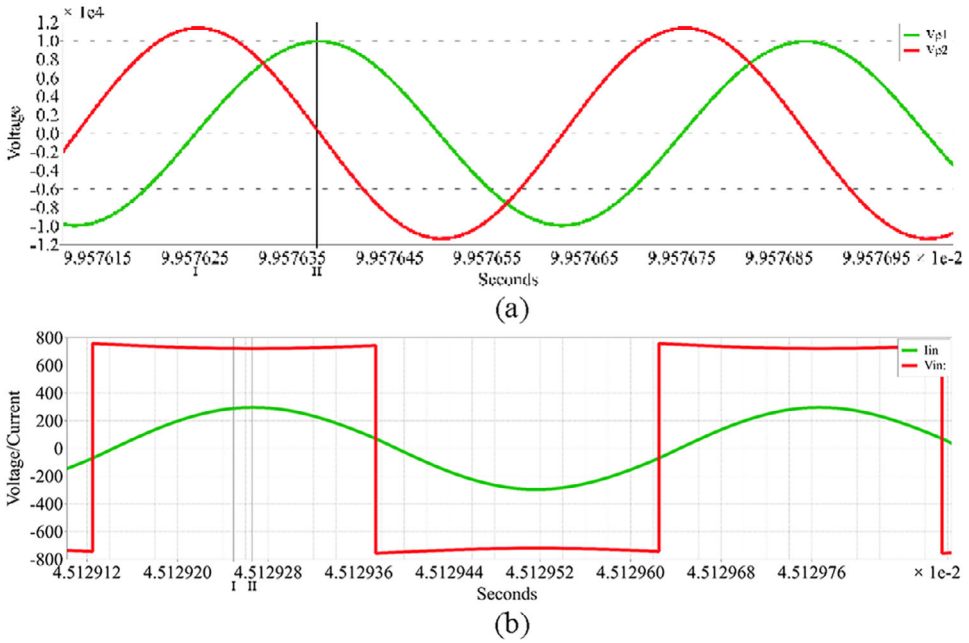

FIGURE 6 (a) Low coupling CPT system plate voltage waveforms, showing phase difference between input and output plate voltage. (b) Low coupling CPT system input voltage and current waveforms, showing unity power factor.

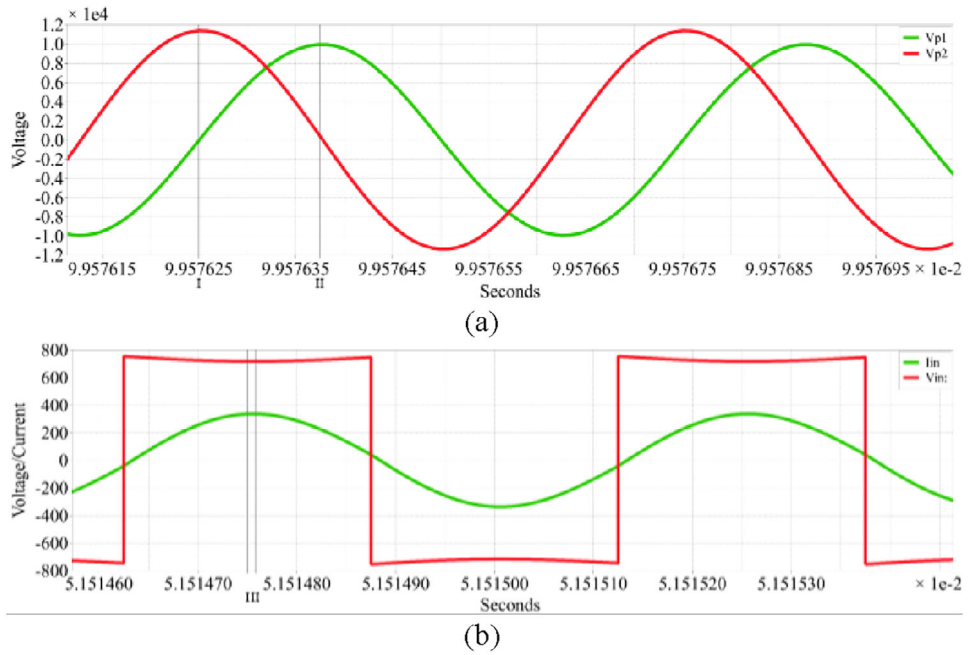

FIGURE 7 (a) High coupling CPT system plate voltage waveforms, showing phase difference between input and output plate voltage. (b) High coupling CPT system input voltage and current waveforms, showing unity power factor.

The housing of the aluminum plates was constructed of 5 mm thick acrylic plastic that extends at least 20 mm beyond the edge of the capacitive plates. These are mounted using a 2-part Epoxy glue with insulative properties, thereby achieving a strong di-electric environment around the aluminum coupler. For the purposes of the downscaled system, the switching frequency is selected as 1 MHz (due to inverter switching limitations), and the capacitor dissipation factor is selected as 0.001 (0.1%), which is derived from WIMA film capacitors found commercially [24]. This model of capacitor imposes a limitation of $700V_{ac}$ on the plate voltage amplitude, which must be adhered to when component values are selected. At this stage,

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TABLE 7 CPT plate structure of downscaled prototype.

Design parameter	Design value
Plate length	140 mm
Plate width	280 mm
Total plate area	39200 mm^2
Thickness	1 mm
Material	Aluminum
Plates per coupling (per bogey)	2
Airgap (Z)	10 mm
Mutual capacitance	36.77 pF

due to unknown inductor sizing, these losses are kept ideal during the optimal power transfer search portion of the design. They are to be calculated following the selection of passive components. The input voltage is reduced to 20 V. Figure 8 shows the results of investigating a stagger-tuned system where the resonant inductors are tuned to achieve a close-to-90° phase shift between the couplers' voltages. From Figure 8a, it is clear that signficiant power transfer is possible when a 20 V input voltage is supplied to a small-scale CPT system. Increasing power delivery is observed as C_{ex1} is increased beyond 1000 pF. However, Figure 8a also highlights that there is a discernible decline in efficiency as the C_{ex1} is increased beyond 1000 pF. Furthermore, Figure 8b indicates that despite maintaining a 90° phase shift between V_{p1} and V_{p2}, the voltage stress on the plates increased beyond 750 V for values of C_{ex1} larger than 1000 pF, breaching the upper voltage limit of the hardware capacitors. As a result, 990 pF for C_{ex1} is selected at which the design requirements (desired power, efficiency, 90° phase angle) are met.

5.1 | Simulated results

At this stage, the inductor losses are calculated using the same method outlined in Section 3.3, with 0.04 mm, 250 strand Litz wire. This resulted in the AC/DC resistance ratio of 1.74, and R_{ac} of 0.0597 Ω/m. A simulation was then conducted on the completed downscaled system. Figure 9a shows the voltage plate profiles of this system, where a 90° phase angle is observed. Figure 9b illustrates the input voltage and current from the inverter and highlights that a near-to-unity power factor is achieved at the input side, resulting in minimized reactive power in the system. A further assessment of resilience to a changing load is conducted, whereby the resistive load is varied away from the design load of 50 Ω. For each load in the range, coupler voltage phase difference and input phase differences are noted. The results of this investigation are included in Figure 10. With variation in the load resistance, there is slight detuning away from the ideal operational condition of 90° phase difference. Finally, the input and output voltages, currents and power values are recorded from the simulated system for comparison to the physical model in the next section. The passive component values selected are detailed in Table 8.

TABLE 8 Designed parameters for matching circuit.

System design parameter	Value
C_{ex1}, C_{ex2}	990 pF, 300 pF
L_1, L_2	25 uH, 74.5 uH
System resonance frequency	1 MHz
Plate structure	2 Plate (Rectangular)
Return path method	Grounded

TABLE 9 CPT system component list and values.

Component	Manufacture part #	Value
Inverter	2 × EVALHBGAN	GaN HEMT, 1 MHz R_{on} = 140 mΩ
Inverter driver	XMC140	VQFN64 MC, 32 kHz to 20 MHz
DC power supply	CPX200DP	180 W Max
Capacitor (LC tank)	Parallel arranged 3 × FKP1T003304B00JSSD 3 × FKP1U001004B00JF00	700V_{ac} 330 pF (5%), 100 pF (5%)
Inductor (LC tank)	Self-wound Litz wire	0.04 mm × 250 strands
Rectification	4 × MUR420, Full Bridge	0.89 V drop
Rectifying capacitor	1 × MKP1839510161	160 V_{dc}, 1 nF (1%)

5.2 | Experimental model and results

The downscale CPT design has been reached following the proposed design algorithm for implementation in a laboratory setting. The inductor values listed in Table 8 are set as the design point for implementation. The LC componentry is mounted into a printed circuit board assembly to reduce resistance and undesirable passive couplings. Furthermore, the external capacitors are constructed from three individual units placed in parallel, with connection points located as close to the capacitor terminals as possible. Table 9 summarizes the components used to build the prototype. Figure 11 shows the system configuration and the laboratory bench set-up.

To verify the physical implementation of the system, assessment of the power delivery to a fixed load was conducted, replicating that of the simulated environment. The power measurement is taken following rectification with a diode bridge and filtering capacitor, across a fixed wire-wound resistor. As shown in Figure 12, the experimental supplied power and delivered power measured by a WT1800 Precision Power Analyzer closely match with the simulation results. Table 10 summarizes both simulation and experimental findings and validates the proposed design and implementation process.

There exists a clear discrepency in the DC-DC efficiency percentage from ERV to downscale system design. Since the simulated and experimental findings match closely, the losses are likely attributable to two key factors: i) the selected power throughput is quite low (40 W), so dissipation in the semiconductor devices is relatively more significant, and ii) due to

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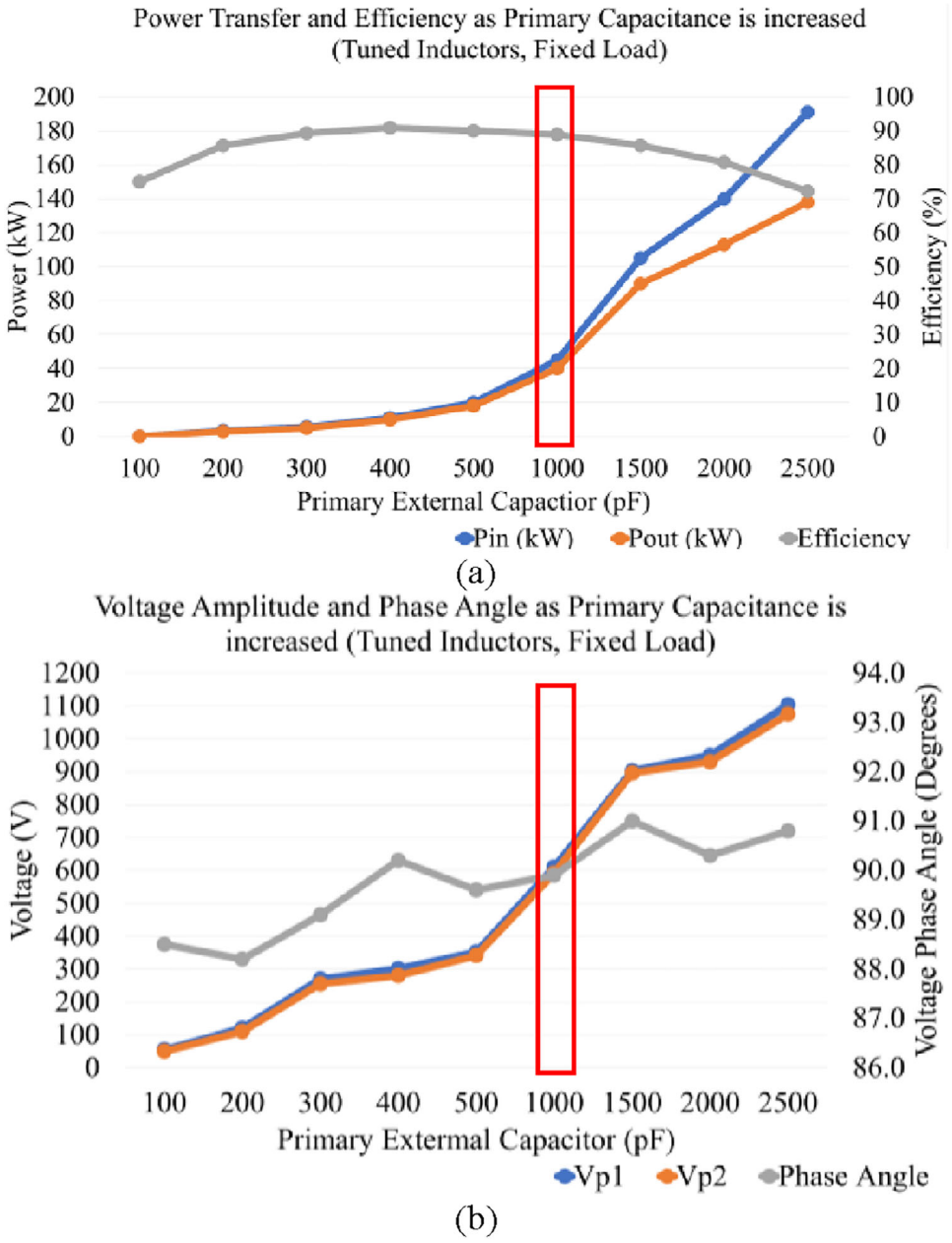

FIGURE 8 (a). Efficiency and power transfer of downscaled system as C_{ex1} is increased and inductors are tuned. (b) Voltage amplitude and phase angle of plate voltages as C_{ex1} is increased and inductors are tuned.

high current present in the matching networks (2–3 A), the losses in the primary and secondary matching inductors are high, indicating the Litz construction of the inductors did not exhibit low resistance. Hence the losses due to high current are excerbated (as evidenced by a R_{ac}/R_{dc} ratio of 1.74). Since the simulated model and physical model are within 10% accuracy, an assessment of the losses in the simulated model reveals the component breakdown of where losses are occuring, as shown in Figure 13.

As expected, the matching inductor coils account for over 70% of the losses present in this system (~10.39 W), with the semiconductor losses (diode bridge and inverter), accounting for a further 16%. This indicates that with a higher power throughput, and optimized inductor construction, a higher efficiency is attainable at this scale. Overall however, the desired system behaviour is preserved, indicating that with further improvements to the physical construction and selection of specialist LC components, higher efficiency results should be achievable.

This reflects that the design process can achieve a physical model that exhibits the desirable qualities for higher power transfer and lower plate voltages in a real implementation. Hence validating that this process is stuiable for the design of a CPT system to meet design specifications, as already

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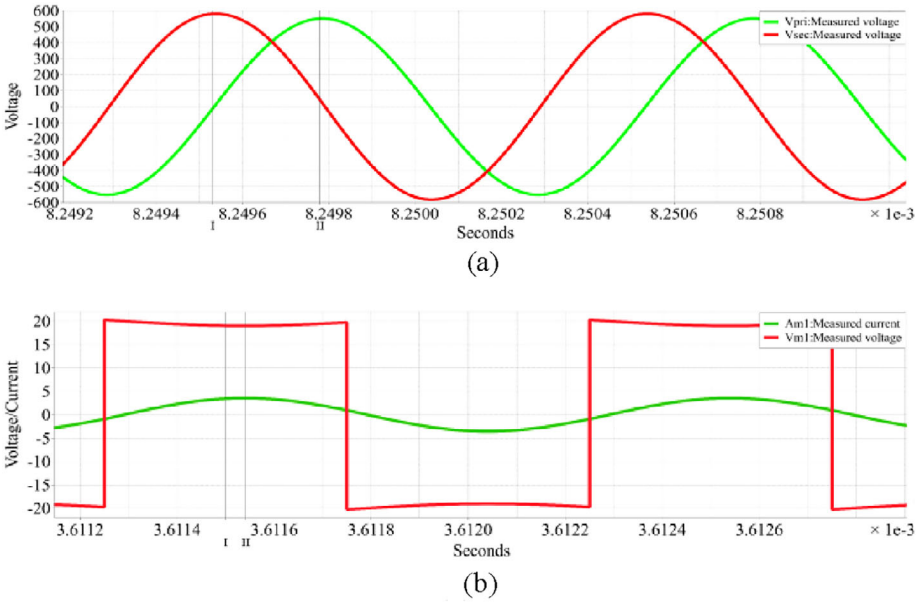

FIGURE 9 (a) Plate voltage profiles showing phase shift in plate voltages. (b) Input voltage and current waveforms operating at close-to-unity.

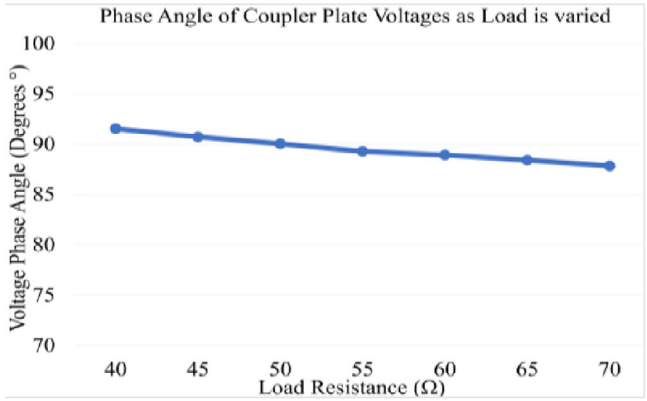

FIGURE 10 Plate voltage phase angle as load is varied around design value.

TABLE 10 Comparison of simulation and experimental findings.

Performance metric	Simulation results	Experimental results	Error
Input voltage	20.00 V	20.01 V	1%
Input current	2.052 A	2.16 A	5%
Input power	41.03 W	43.36 W	6%
Load voltage	39.14 V	39.10	1%
Load current	0.78 A	0.781	1%
Output power	30.64 W	30.5 W	1%
Efficiency	74.68%	70.43%	6%
Primary plate voltage (RMS)	366 V	402 V	8%
Secondary plate voltage (RMS)	411.5 V	412 V	1%
Plate voltage phase angle (θ)	90.23°	90.1°	1%

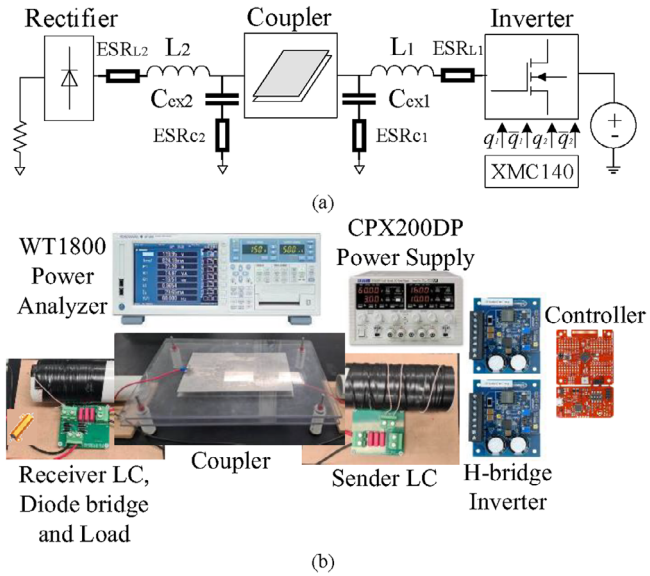

FIGURE 11 System configuration and the laboratory bench set-up.

presented in Section 2. Figure 14 demonstrates the primary plate voltage in blue and secondary plate in yellow, as well as the time difference of 250 ns observed with the oscilloscope cursor functionality, verifying a 90°-degree phase shift (at 1 MHz) between the coupler voltages. Figure 15 shows input voltage (blue) and input current (yellow) waveforms. It is clear that the waveforms match closely with the simulation results. The near-to-unity power factor at the input, and 90° phase shift in coupler voltages offered by a stagger-tuning approach are therefore observed in both simulation and physical implementation, which verifies the effectivenss of the proposed design approach.

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FIGURE 12 Experimental power profile of CPT system using WT1800 Precision Power Analyzer.

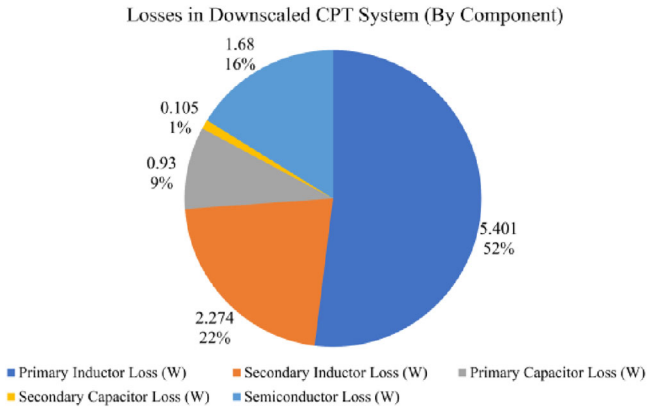

FIGURE 13 Losses breakdown by component.

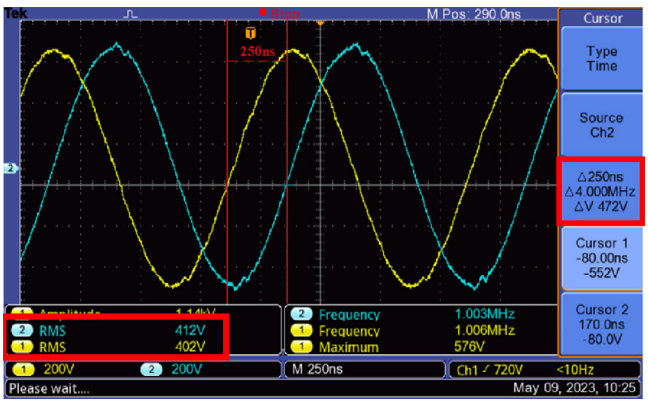

FIGURE 14 Plate voltage profiles and phase angle.

6 | CONCLUSION

A novel algorithm for designing stagger-tuned matching networks for CPT systems was presented. The demonstrated algorithm enables a simple double-sided LC matching CPT network to achieve over 100 kW of power at high efficiency (~90%), whilst minimizing voltage stress on the coupler plates by regulating the couplers' voltage phase angle to approach 90°.

FIGURE 15 Phase angle of input voltage and current.

This achievement reduces the risk of breakdown voltage and safety concerns in the vicinity of public CPT applications, for example, ERVs. To validate this design methodology, which considers real-world limiting factors such as ESR and the market availability of passive components, a downscaled laboratory prototype is developed and tested under the same operational conditions as the simulated system.

AUTHOR CONTRIBUTIONS

Kyle John Williams: Conceptualization; investigation; methodology; writing—original draft. **Graham Town**: Conceptualization; methodology; supervision; writing—review and editing. **Sara Deilami**: Supervision; validation; writing—review and editing. **Foad Taghizadeh**: Conceptualization; methodology; project administration; supervision; validation; writing—original draft; writing—review and editing.

CONFLICT OF INTEREST STATEMENT

The authors declare no conflicts of interest.

DATA AVAILABILITY STATEMENT

Data sharing is not applicable to this article as no new data were created or analyzed in this study.

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