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**This is the accepted author manuscript version of an article published as:**

Callegaro, L., Ciobotaru, M., & Fletcher, J. E. (2019). An intelligent pass-through algorithm for non-inverting buck-boost solar power optimizers. In *2019 21st European Conference on Power Electronics and Applications (EPE '19 ECCE Europe)* (pp. 1-10). Institute of Electrical and Electronics Engineers (IEEE).

**Access to the published version:** <https://doi.org/10.23919/EPE.2019.8915459>

# An Intelligent Pass-Through Algorithm for Non-Inverting Buck-Boost Solar Power Optimizers

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## Keywords

«Converter control», «Renewable energy systems», «Distributed power», «Digital control», «Non-inverting buck-boost converter»

## Abstract

The non-inverting buck-boost is a converter topology commonly encountered in renewable energy applications, as it is able to provide a wide range of output voltages, while its input voltage can be regulated to extract the maximum power available from the source. When input and output voltage of this converter are in close proximity, special dead-zone avoidance controls must be activated, in order to achieve stable operation. Abundant literature documents detrimental effects of the dead-zone, deemed to cause uncontrollability, increased ripple and sub-harmonic oscillations in the regulated voltage.

This paper proposes a new algorithm to avoid the operational dead-zone in the non-inverting buck-boost converter by introducing a pass-through operation. In this mode, the input port is directly linked to the output port of the converter, avoiding pulse width modulation (PWM) switching, whenever the voltage at these two ports is within a narrow range. Existing dead-zone avoidance techniques rely on using extra switches, or on using a buck-boost operation which inevitably increases the conversion losses. Conversely, the proposed technique does not rely on simultaneous buck and boost PWM operation and does not need additional hardware to activate the pass-through mode. The presented control algorithm is thoroughly discussed and implemented in a digital microcontroller. Finally, efficiency measurements and experimental results executed on a 200 W non-inverting buck-boost photovoltaic module integrated converter are used for performance evaluation.

## Introduction

While it is common to think of photovoltaic (PV) energy systems as strings of PV modules connected to one or more inverters, micro-converters installed in each PV module (Fig 1a) and known as dc-module integrated converters (dc-MICs), or power optimizers, are also being increasingly adopted. Among the benefits of these so-called PV module-level converters, emerge the increase in solar energy harvest, and the mitigation of losses otherwise caused by partial shading and mismatching [1].

In the configuration of Fig. 1a, the output voltage of a dc-MIC assumes a wide range of values depending on the processed PV power and the dc-link voltage [2], framing the non-inverting buck-boost converter as an optimal topology for this task. This converter is shown in Fig. 1b, its operating principle being explained in [3, 4]. Ideally, the buck ( $d_1 \neq 0, d_2 = 0$ ) or boost ( $d_1 = 1, d_2 \neq 0$ ) operation alone would satisfy the requirement to meet a wide range of output voltage values. In practice, dead-time imposed on PWM gating signals and minimum switch on-time constraints [5, 6] limit the converter duty-cycles,

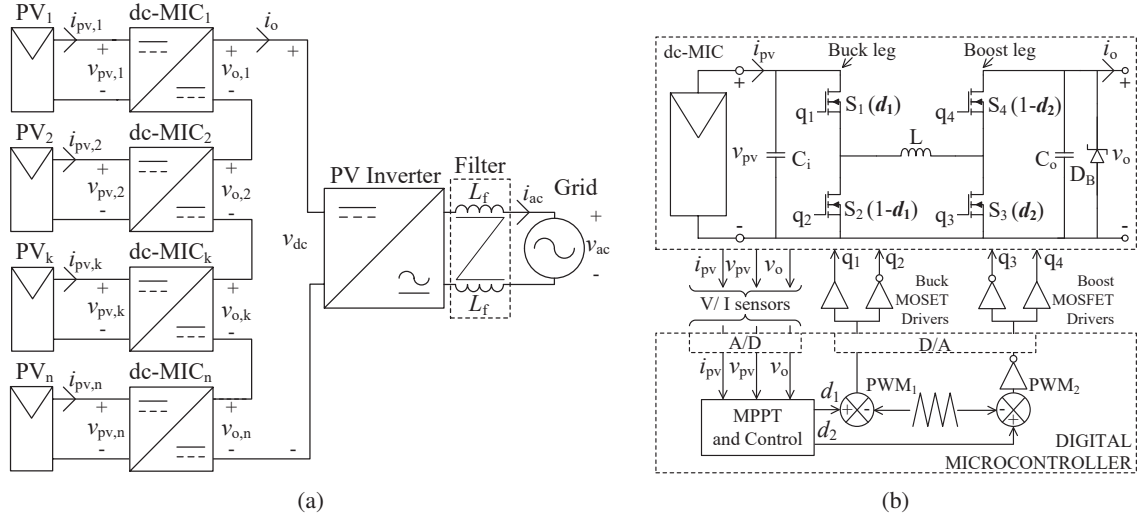


Fig. 1: (a) PV string equipped with dc-MICs. (b) dc-MIC power and control stage

and thus the achievable output voltage, in the buck or boost mode alone. This limitation causes an operational dead-zone [4, 6] occurring when the converter output voltage is in close proximity, or equal, to the input voltage. Without an appropriate duty-cycle control strategy, operation of the non-inverting buck-boost converter close to unity voltage gain would cause loss of regulation, increased voltage ripple, sub-harmonic oscillations and instability [6].

In the literature, several strategies are devised to avoid the dead-zone and its associated problems. Other than by simultaneous switching of both buck and boost leg, used in [4, 5, 6], which comes with the disadvantage of increased switching losses, the dead-zone can be avoided if the converter input and output ports are directly connected. Referring to Fig 1b, this is done by closing the high-side switches ( $S_1$ ,  $S_4$ ), whilst leaving the low-side ones open ( $S_2$ ,  $S_3$ ). This operational mode, known as “pass-through”, was firstly discussed in [5, 7], albeit without delving into any detailed analysis. In [8], a possible pass-through implementation is described, notwithstanding the disadvantage of using two additional switching devices for the purpose. In summary, the pass-through mode implementation is treated rather superficially in today’s literature, which lacks discussion of suitable algorithms, or proposes to adopt additional hardware for the task, unnecessarily increasing costs.

This paper aims to address these gaps. Firstly, a detailed control algorithm achieving the pass-through mode (without additional switches) is designed and implemented. Secondly, it is presented a comparison between the converter efficiency when the proposed pass-through algorithm is applied and when simultaneous buck and boost PWM switching is adopted. In the next section, the reasons behind the operational dead-zone in the non-inverting buck-boost dc-MIC are briefly reviewed. Attention is then devoted to describe the proposed pass-through algorithm, with a framework for microcontroller implementation. Experimental results drawn from a 200 W dc-MIC prototype demonstrate the proposed pass-through functionality in practice. Finally, conclusions and plans for future work will close the manuscript.

## Operational constraints for the non-inverting buck-boost dc-MIC

Minimum on-time required by MOSFETs and dead-time introduced in the gating signals to avoid shoot-through limit the maximum buck mode and minimum boost mode duty-cycle. Fig. 2 visualises this limitation, by displaying the PWM gating signal of a generic switching leg.

It is simple to deduce the maximum buck duty-cycle,  $d_{1,max}$ , and the minimum boost duty-cycle,  $d_{2,min}$ , within a switching period  $T_{sw}$ :

$$d_{1,max} = 1 - \frac{2\Delta t + t_{on(min)}}{T_{sw}}, \quad d_{2,min} = \frac{t_{on(min)}}{T_{sw}}. \quad (1)$$

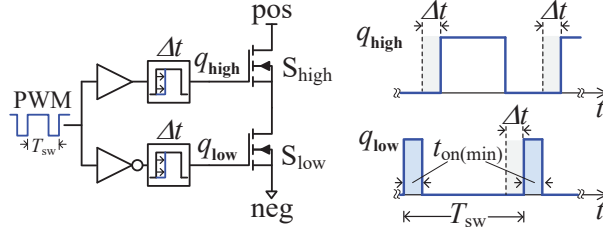


Fig. 2: Gating signals for a generic switching leg, with  $t_{\text{on}(\text{min})}$  minimum switch on-time and  $\Delta t$  dead-time imposed by the gate driver

With the dc-MIC voltage gain,  $G$ , defined as the ratio between the converter output and input voltage, i.e.  $G = \frac{v_o}{v_{\text{pv}}}$ , then according to the limitations posed by (1), the maximum converter gain in buck mode and the minimum converter gain under the boost mode are respectively:

$$G_{1,\text{max}} = d_{1,\text{max}}, \quad G_{2,\text{min}} = \frac{1}{1 - d_{2,\text{min}}}. \quad (2)$$

Whenever  $v_o$  is in close proximity to  $v_{\text{pv}}$ , the converter voltage gain happens to be  $G_{1,\text{max}} < G < G_{2,\text{min}}$ , and either the buck leg would be required to operate a  $d_1 > d_{1,\text{max}}$ , or the boost leg at  $d_2 < d_{2,\text{min}}$ . As these modes are not possible, special control methods are devised to overcome this limitation and the problems associated with it, as mentioned in the Introduction. In summary, additionally to the buck (Fig. 3a) and boost mode (Fig. 3c), this paper proposes to adopt a new pass-through mode (Fig. 3b), whose details are disclosed in the next section.

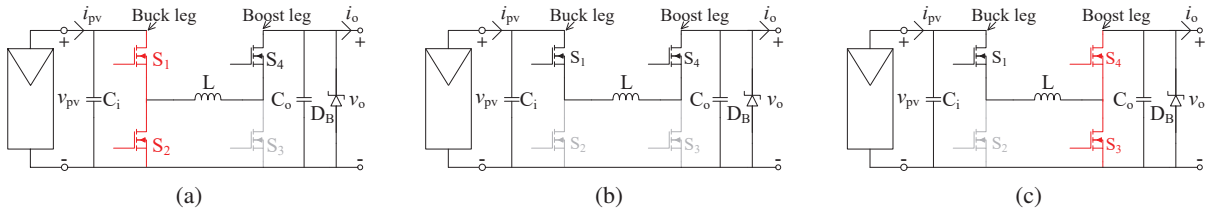


Fig. 3: dc-MIC operating modes (red colour: switch in PWM operation; black colour: switch permanently closed; grey colour: switch permanently open). (a) Buck mode: when  $v_{\text{pv}} > v_o$ . (b) Pass-through mode: when  $v_{\text{pv}} \approx v_o$ . (c) Boost mode: when  $v_{\text{pv}} < v_o$

## Proposed pass-through control algorithm

### Overview

The dc-MIC digital control algorithm is composed of two main loops: a background loop (Fig. 4a) running continuously, and a fast interrupt service routine (ISR, Fig. 4b), whose execution rate is the converter switching frequency  $f_{\text{sw}}$ . The background loop comprises the perturb and observe (P&O) maximum power point tracking (MPPT) algorithm updated at  $f_{\text{mppt}} = 10$  Hz. The P&O was chosen because of its simplicity.

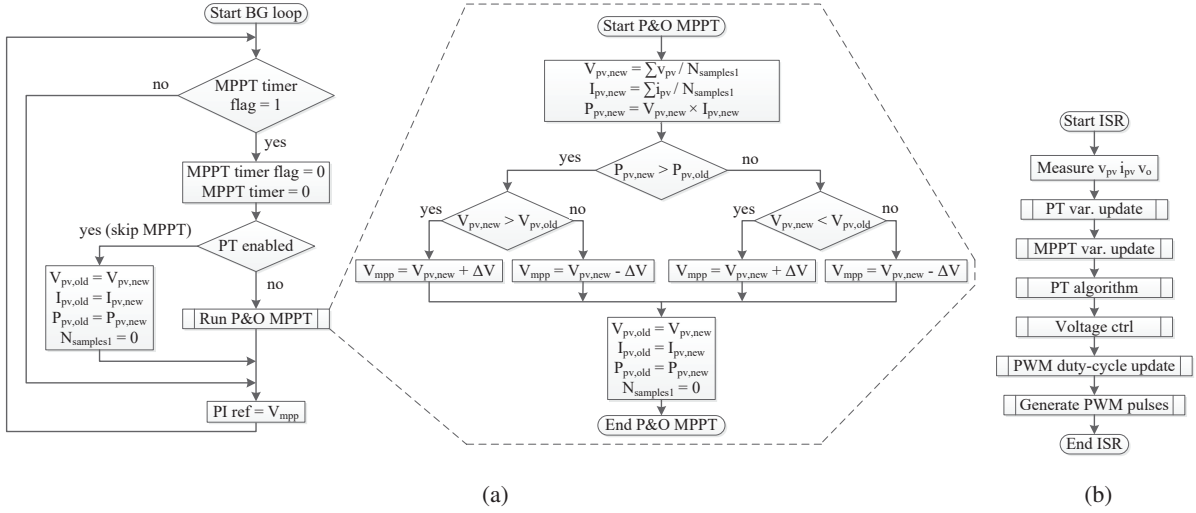


Fig. 4: Overview of the digital control algorithm. (a) Background loop, comprising MPPT calculation. (b) Interrupt service routine (each square block representing a sub-process)

### Detail of each ISR sub-process

The key functions of the proposed algorithm are revealed in the sub-processes included in the ISR of Fig. 4b. After measurement of voltage ( $v_{pv}$ ,  $v_o$ ) and current ( $i_{pv}$ ) of interest, each ISR sub-process is articulated below, according to the flowcharts of Fig 5.

*Pass-through variables update* (Fig. 5a): if the pass-through timer reached the set limit, the dc-MIC voltage gain is calculated as the ratio between the average output voltage and the latest MPP voltage given by the P&O algorithm.

*MPPT variables update* (Fig. 5b): in this sub-process, if the MPPT timer has reached a preset time value, the MPPT timer flag is set to one. This flag is read in the background loop program (Fig.4a), and if the pass-through mode is not enabled, the P&O algorithm is run, or otherwise it is skipped.

*Pass-through algorithm* (Fig. 5c): on the left-hand side, the decision regarding entering the pass-through mode is made. If the dc-MIC voltage gain calculated in the sub-process of Fig. 5a is higher than the maximum gain under buck mode, or is lower than the minimum gain under boost mode, then the pass-through mode is enabled, and in turn the voltage controller is disabled. The right-hand side of Fig. 5c deals with the decision to exit the pass-through mode and resume buck, or boost, and MPPT operation. In this case an hysteresis,  $h$ , is considered in the comparison between the dc-MIC voltage gain calculated in the sub-process of Fig. 5a and the maximum buck/minimum boost voltage gain. The hysteresis avoids abrupt mode change from buck or boost to pass-through and vice versa. Note that the dc-MIC operation shall return to buck mode or boost mode if  $G_{1,max} - h > G > G_{2,min} + h$ . Assuming that one of the condition above is true, if the pass-through enable bit is set to one, meaning a previous pass-through operation, then the voltage controller is switched back on, and the pass-through exit flag is set to one, signalling that the pass-through mode is disengaged. Afterwards, the pass-through enable bit is set to zero.

*Voltage control* (Fig. 5d): this is where the PI controller is executed, or not, depending on the decision made by the *pass-through algorithm* sub-process of Fig. 5c. Note that PI controller old output state is reset to zero if the voltage controller is disabled. If the pass-through exit flag is set to one from the sub-process of Fig 5c, then it is the first time that the voltage control algorithm is reactivated, following a previous pass-through operation mode. Consequently, the reference voltage input to the PI controller is set as the measured PV voltage (PI ref =  $v_{pv}$ ), because during pass-through mode the MPPT algorithm is not executed. Moreover, this sub-process understands if the dc-MIC operation must return to boost ( $v_o > v_{pv}$ ), or to buck ( $v_o < v_{pv}$ ), and tries to achieve a smooth mode transfer by setting the PI output either

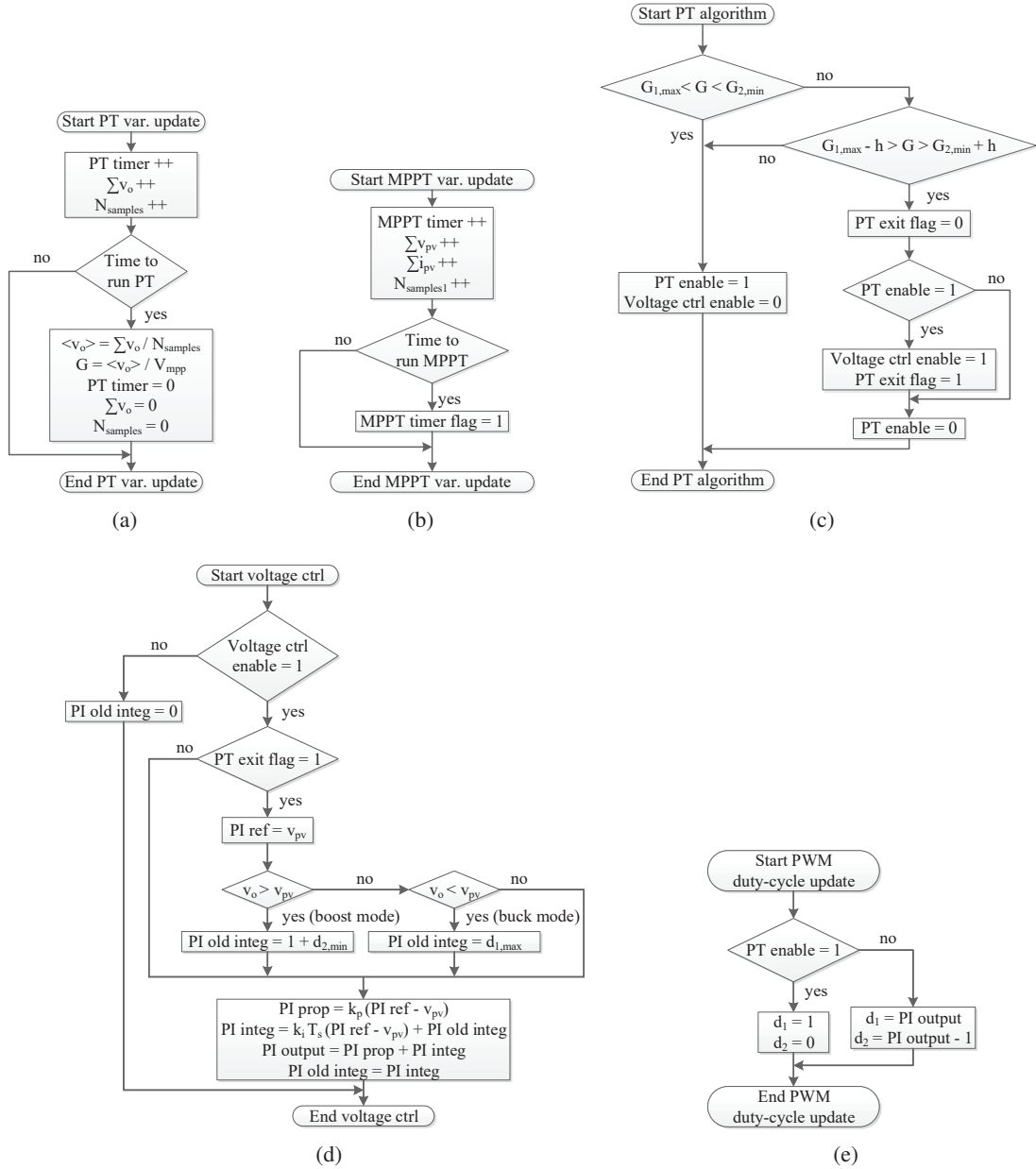


Fig. 5: ISR key sub-processes. (a) Pass-through variables update. (b) MPPT variables update. (c) Pass-through algorithm. (d) Voltage control. (e) Duty cycle update

to  $1 + d_{2,min}$ , or  $d_{1,max}$ , respectively. This choice is dictated by the assumption that the return to buck or boost operation occurs with the dc-MIC operating with close values of  $v_{pv}$  and  $v_o$ . Afterwards, the PI controller algorithm is executed using the backward-Euler [9, p. 53] formula. An integrator anti-windup calculation [10, p. 655] (omitted in the picture) may also be executed.

*Duty cycle update (Fig. 5e):* the last sub-process updates the duty cycle  $d_1$  and  $d_2$  supplied to the buck and boost leg PWM modulators. If the pass-through mode is enabled, then only the high side MOSFETs are switched on, attained by setting  $d_1 = 1$  and  $d_2 = 0$ . Otherwise,  $d_1$  and  $d_2$  are set according to the modulation scheme determining the independent buck or boost operation (e.g. see [6]).

Overall, the proposed algorithm achieves a reliable transfer between the dc-MIC operating in the buck or boost mode, and the pass-through mode, whenever input and output voltage are in close proximity.

## Experimental Results

A dc-MIC prototype was designed and built and was interfaced to a custom-designed control board, through which the converter interacts with the digital microcontroller. Table I summarises data relevant to the dc-MIC prototype, while Fig. 6 displays the converter and control platform.

Table I: Relevant dc-MIC and microcontroller specifications

	Value or ratings	Notes
Inductance	$L = 22 \mu\text{H}$	Coilcraft AGP4233
Input Capacitance	$C_i = 110 \mu\text{F}$	Ceramic X7S
Output Capacitance	$C_o = 2.4 \mu\text{F}$	Ceramic X7R
Switching frequency	$f_{\text{sw}} = 200 \text{ kHz}$	$T_{\text{sw}} = 5 \mu\text{s}$
MOSFETs	150 V/100 A	Infineon IPP075N15N3G
Gate drivers	118 V bootstrap supply 1.2 A source/1.8 A sink	Texas Instruments LM5106
Microcontroller	PWM resolution 100 MHz	Texas Instruments TMS320F28377D

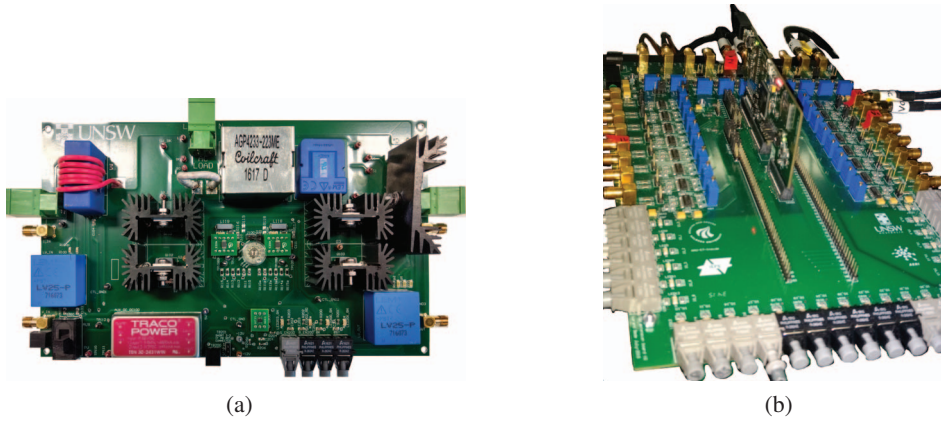


Fig. 6: Custom-designed and built elements of the experimental setup. (a) Non-inverting buck-boost converter. (b) Control platform including digital microcontroller

### Functionality validation of the proposed algorithm

This experiment was carried out on a single dc-MIC. The converter was fed by a PV emulator (*Regatron TopCon Quadro TC.P* with *TC.LIN* post-processing unit) emulating the  $i$ - $v$  characteristic of a 100 W crystalline silicon PV module, with MPP at 26 V. The PV power converted was transferred to an electronic dc load (*Kikusui PLZ1004WH*), operating in the constant voltage mode. The output voltage on the electronic load was programmed to vary, so that its value went above and below the MPP voltage. In this way the dc-MIC was forced to operate in all available modes, that is buck, boost and pass-through mode. A *LeCroy HDO4054* digital oscilloscope was used to display the waveforms of interest.

Fig. 7a portrays the waveforms of the output voltage (pink) and input voltage (blue) as measured by the dc-MIC sensors. The load voltage varies from 15 V to 35 V, while the dc-MIC input voltage is either following the reference calculated by the P&O algorithm, or the output voltage waveform when the pass-through mode is active. In Fig. 7b the dc-MIC operation transits from buck mode where  $v_o$  (pink waveform) is smaller than  $v_{\text{pv}}$  (blue waveform), to pass-through mode having  $v_o \approx v_{\text{pv}}$  and finally to boost mode where  $v_o$  is greater than  $v_{\text{pv}}$ . Fig. 7c displays the change in the dc-MIC operation from boost mode ( $v_o > v_{\text{pv}}$ ), to pass-through mode ( $v_o \approx v_{\text{pv}}$ ) and finally to buck mode  $v_o < v_{\text{pv}}$ , with analogous considerations as for Fig. 7b. The engagement and disengagement of the pass-through mode occur smoothly, without causing large transients to the dc-MIC input voltage.

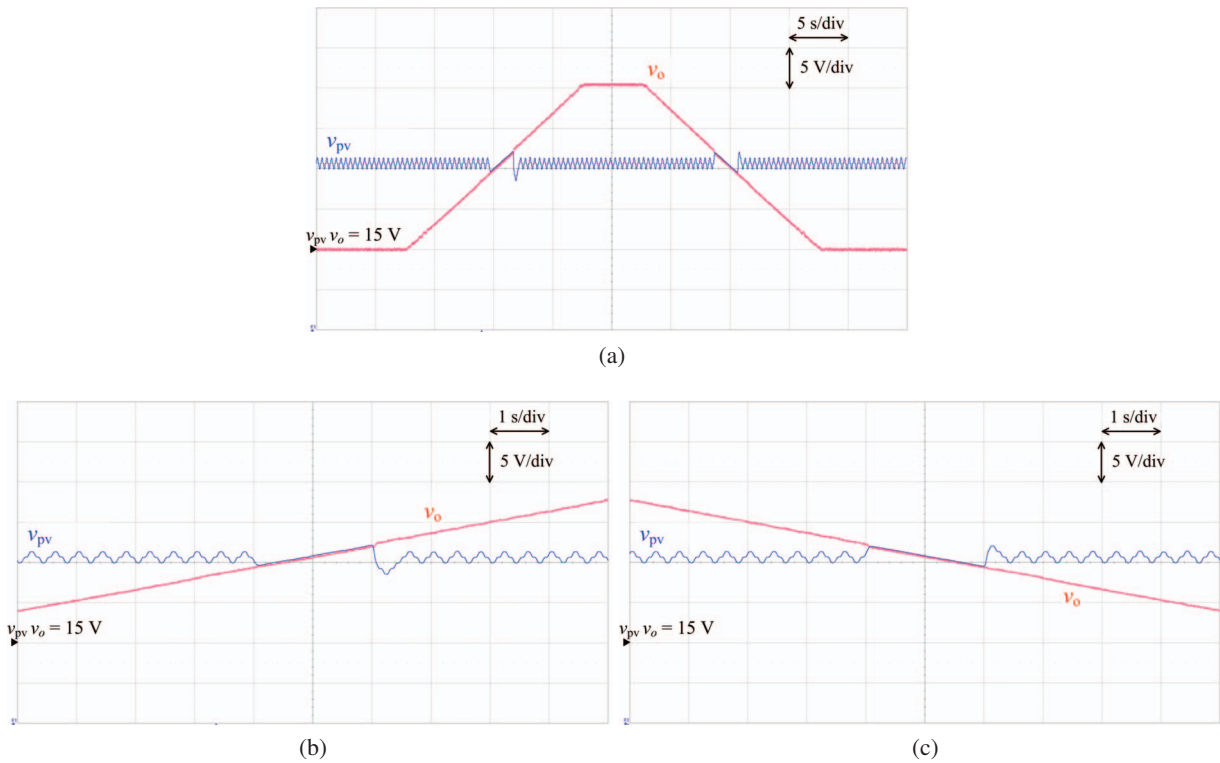


Fig. 7: Pass-through algorithm validation test on one dc-MIC. (a) Output voltage variation profile (pink) vs. PV voltage (blue). (b) Buck/pass-through/boost mode transition. (c) Boost/pass-through/buck mode transition

### Power harvest and efficiency measurements

In this test the output voltage on the dc-MIC was varied in small increments while the input voltage was held constant and equal to the PV module rated MPP voltage. This choice eliminates the input power and voltage variability associated with the dithering behaviour of the MPPT algorithm. The hardware setup was the same used in the previous experiment, except for the addition of a *Yokogawa WT3000* power analyser. This was used to measure the dc-MIC output power and power-stage efficiency at each value of output voltage around the MPP voltage.

In Fig. 8, the results obtained with the proposed control algorithm are compared with the results given by

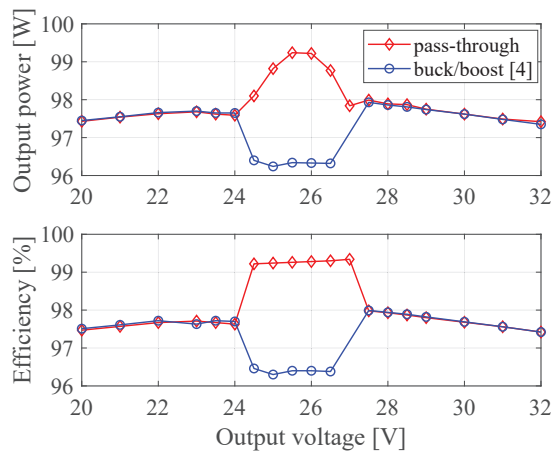


Fig. 8: dc-MIC output power (top) and power-stage efficiency (bottom) for varying output voltage values  $v_o$ , with constant input voltage  $v_{pv} = 26$  V, excepted during pass-through operation when  $v_{pv}$  follows  $v_o$



the algorithm presented in [4], which by contrast adopts a simultaneous buck and boost PWM operation when the dc-MIC input and output voltage fall within a close range. Note that on the left and right-hand side of the plots in Fig 8, the dc-MIC is respectively operating in buck or boost mode alone, as its input voltage is regulated to 26 V by the input voltage controller. Useful information emerges from the middle section of each plot. The output power harvest, displayed at the top of Fig. 8, clearly shows an improvement when the pass-through mode is active. Here, the output power curve follows the  $p$ - $v$  curve profile of the PV module. Conversely, with the technique of [4], the output power drops because of increased switching losses given by the simultaneous PWM operation of the buck and boost legs of the dc-MIC. Likewise, the converter power stage efficiency, bottom plot in Fig. 8, shows an increment when the proposed pass-through mode is active. Increased switching losses, obtained with the comparison technique from [4], diminish the conversion efficiency when input and output voltage are approximately equal.

### Results with multiple series-connected converters

This experiment was performed with two series-connected dc-MICs, to reflect the configuration of Fig. 1a. A constant voltage electronic load was used instead of the grid-connected inverter. The inverter would regulate the dc-link voltage to a constant reference value, therefore it was considered appropriate to emulate this effect by a constant voltage load. The schematic of the setup is displayed in Fig. 9.

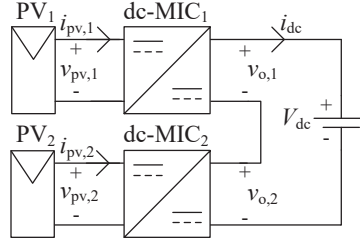


Fig. 9: Schematic of the experimental setup used to evaluate the behaviour of series connected dc-MICs

It is assumed that the dc-link reference voltage is  $V_{dc} = 52$  V, i.e. the rated MPP voltage,  $V_{mpp}$ , times the number of series connected (via dc-MIC) PV modules,  $n$ , that is:  $V_{dc} = V_{mpp} \times n$ . Under this assumption, shall the solar irradiation on each PV module be equal, then both dc-MICs are working in the pass-through mode. When there is an irradiance mismatch, each dc-MIC would be working in the buck or boost mode, with output voltage determined by the relation [2]:

$$v_{o,k} = V_{dc} \frac{P_{pv,k}}{\sum_{i=1}^n P_{pv,i}} \quad (3)$$

where, disregarding losses from simplicity,  $P_{pv,k}$  is the PV power transferred to the load by the  $k$ -th PV module in the string.

In the first experiment, whose waveform are represented in Fig. 10, both dc-MICs are initially working in the pass-through mode. After the 1 s time-mark, the solar irradiation on PV module 2 is decreased from  $1000 \text{ W/m}^2$  to  $500 \text{ W/m}^2$ , at a rate of  $100 \text{ W/m}^2\text{s}$ . While the input voltage of each dc-MIC remains about the PV module MPP voltage (remembering that the MPP voltage is only weakly sensitive to solar irradiation change), the output voltage of dc-MIC<sub>1</sub> increases, whereas the output voltage of dc-MIC<sub>2</sub> decreases, in accordance with (3). From Fig. 10, it is apparent that the MPPT algorithm starts as soon as the pass-through mode is disengaged, as intended by the designed algorithm.

In Fig. 11 the dc-MIC waveforms are represented when the solar irradiation on PV module 2 returns from  $500 \text{ W/m}^2$  to  $1000 \text{ W/m}^2$ . Operation of dc-MIC<sub>1</sub> moves from boost to pass-through (Fig. 11a), while dc-MIC<sub>2</sub> goes from buck to pass-through mode (Fig. 11b). Compared to Fig. 10a, the pass-through interval seems to last for a shorter time than in Fig. 11a. This is attributed to the hysteresis band, discussed in Fig. 5c, introduced to avoid repeated mode changes when the dc-MIC is about to exit the pass-through mode.

Finally, in Fig. 10b and Fig. 11b, it is visible a change in the behaviour of the MPPT reference of dc-MIC<sub>2</sub> during the transient. This is caused by the irradiance variation occurring on PV module 2, and the P&O algorithm moving to the new MPP at the different irradiance. After the irradiance transient has elapsed, the MPPT on dc-MIC<sub>2</sub> re-assumes the optimal behaviour (as intended in [11, p. 83]) where the steady-state MPPT voltage reference consists of three points, one in the MPP and two on its sides.

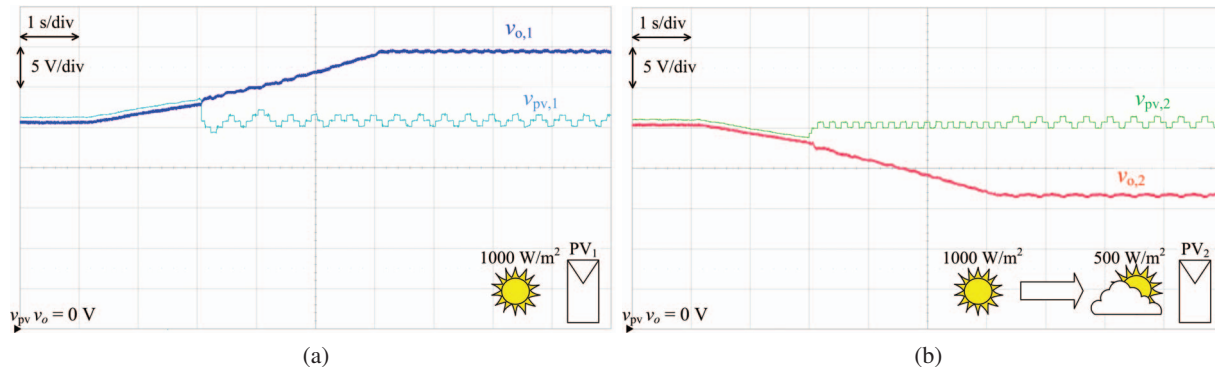


Fig. 10: Effect of irradiation drop on the PV module connected to dc-MIC<sub>2</sub>. (a) dc-MIC<sub>1</sub> waveforms (transition pass-through to boost). (b) dc-MIC<sub>2</sub> waveforms (transition pass-through to buck)

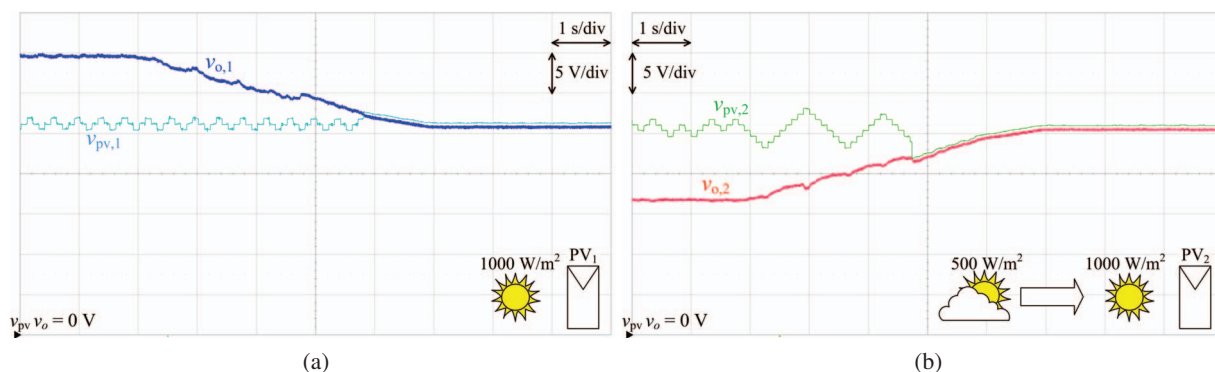


Fig. 11: Effect of irradiation on the PV module connected to dc-MIC<sub>2</sub> returning to 1000 W/m<sup>2</sup>. (a) dc-MIC<sub>1</sub> waveforms (transition boost to pass-through). (b) dc-MIC<sub>2</sub> waveforms (buck to pass-through)

## Conclusions

This paper proposed a pass-through technique to directly link the input to the output port of a PV module integrated converter and transfer power without PWM processing, whenever the converter input and output voltage are in close proximity. A framework to implement the proposed technique in a microcontroller was thoroughly discussed.

Experimental results on a non-inverting buck-boost converter showed the automatic engagement and disengagement of the designed pass-through mode. The power harvest and the converter efficiency have been measured in two cases: when the proposed pass-through mode is implemented, and when simultaneous PWM switching of both converter legs is enforced. The pass-through mode was shown to improve power transfer and increase the conversion efficiency.

Finally, experiments with two converters connected in series were carried out, and the behaviour of the proposed pass-through technique was tested during solar irradiation transients. The algorithm demonstrated again to operate as planned. Future work will focus on fine tuning the proposed pass-through technique and improvement of the MPPT behaviour during solar irradiation transients, as it affects the engagement and release of the pass-through mode.

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