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Feedback Linearization Control in Photovoltaic Module Integrated Converters

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***Abstract*—The strive to increase the energy yield of photovoltaic (PV) power systems has made PV module integrated dc-dc converters (dc-MICs) a reality of modern PV plants. These converters regulate their input voltage, and their dynamic behavior is heavily influenced by the non-linear characteristic of the PV module. The regulation of the PV module voltage and average inductor current by means of a linear cascaded controller is a popular control technique, simplifying the converter dynamics and providing inherent current limiting, however it is prone to instability depending on the interaction between the PV source and the interfacing converter, as well as the value of the controller parameters. These factors present a clear challenge for control design; moreover, the converter transient response undesirably depends on the PV module operating point. In order to solve these issues, while maintaining regulation of PV module voltage and average inductor current, this paper proposes to adopt a non-linear controller designed with the feedback linearization control (FLC) technique. The control laws are derived and implemented in a non-inverting buck-boost dc-MIC, as this is a favorite topology for the PV interfacing application. A digitally controlled converter prototype is built and used to obtain experimental results, where the FLC technique is compared with a linear cascaded control technique. The results confirm the superior performance of the presented FLC technique, which is robust and able to regulate the converter input voltage with fast and consistent dynamics, regardless of the PV module or load operating conditions.**

***Index Terms*—photovoltaic power systems, dc-dc power converters, non-inverting buck-boost converter, nonlinearities, transient response.**

I. Introduction

ADVANCED photovoltaic (PV) power systems are witnessing a technological breakthrough with the adoption of power electronic converters on a per-PV module basis. These devices, also known as PV module integrated converters (MICs), feature maximum power point tracking (MPPT) capability, and have been primarily introduced to increase energy harvest, overcoming the negative effects of partial shading and module mismatching [1], [2]. Micro-inverters, or ac-MICs, are the means to directly connect each PV module to the grid, removing altogether the need for a central PV inverter. ac-MICs demand a high step-up (voltage) ratio and galvanic isolation, resulting in costly components and high efficiencies challenging to achieve. On the other hand, micro-converters, also known as dc-MICs or power optimizers [3], are connected to each PV module and their outputs are series-connected to feed a PV inverter. Albeit the dc-MIC solution still requires a PV inverter, dc-MICs can be implemented using low voltage rated components and without galvanic isolation, yielding higher efficiencies and superior performance over the micro-inverter solution [4], resulting in improved economic attractiveness. The output voltage of a dc-MIC assumes a wide range of values above and below the PV module maximum power point (MPP) voltage, as seen in [5, eq. (22)], thus requiring a buck-boost topology [4]. Therefore, the non-inverting buck-boost converter (Fig. 1) is highly regarded in the dc-MIC application and it is studied in this paper, devoting attention to its control method.

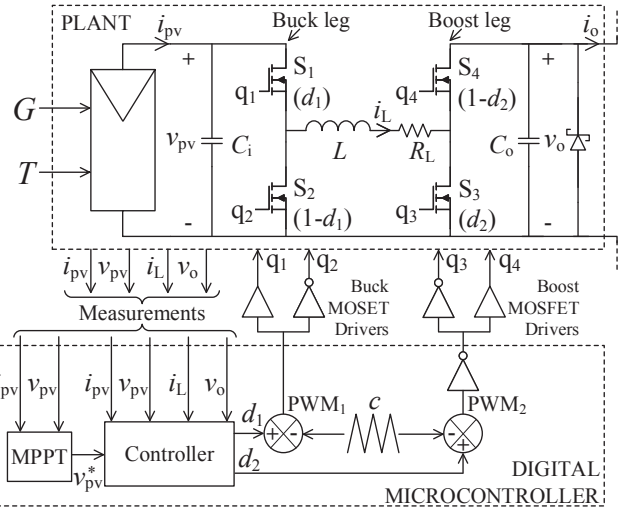

Fig. 1. Non-inverting buck-boost dc-MIC power and control stage, connected to a PV module. G is the solar irradiation and T the temperature on the PV module. q_1 to q_4 are the pulsed width modulated switching functions. d_1 and d_2 are the buck and boost duty cycle, respectively.

In the PV interfacing application, dc-dc converters controlled by linear controllers are especially challenged by the highly non-linear nature of the PV source, manifested by means of its dynamic resistance [6]–[12]. This parameter is subject to wide variations, depending on environmental factors and electrical operating point in the PV module *i-v* characteristic, complicating the design of the linear controller [7], [8]. Properties of the PV generator as an input source for power electronic converters are well documented in [10]. Compared

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to voltage mode control, the linear cascaded control scheme, is a popular method to drastically simplify the controller design [13], [14], despite the variations of dynamic resistance. In the cascaded control scheme, an outer loop regulates the converter input voltage, i.e. the PV module voltage, and an inner loop regulates the average inductor current, inherently providing desirable current limiting features [14]. The linear cascaded control scheme has been studied for the buck, [14]–[16], and boost, [17], [18], PV interfacing converters. Notwithstanding the above-mentioned benefits, with the linear cascaded control scheme, the dc-MIC transient performance remains dependent on the PV module operating region. Even worse, due to the interaction between the PV module and the switching converter, instability may arise in the buck mode, when the PV source operates where its electrical *i-v* characteristic resembles a constant current source [14]–[16]. This issue mandates specific actions in the design of the outer loop controller, regulating the PV module voltage, bringing complexity back into the design process.

This paper proposes an alternative approach to modeling and controller design for the PV interfacing non-inverting buck-boost converter, based on the input/output feedback linearization control technique (hereafter referred to as FLC). By means of this technique, a non-linear controller is designed, solving the above-mentioned issues occurring when a linear cascaded controller is used. Namely, it is shown that with FLC the converter transient performance becomes independent of the system operating point, thus reducing the impact of the PV generator non-linear *i-v* curve. Furthermore, it is demonstrated that the potential instability issue arising when the converter operates in the buck mode, with the PV source in the constant current region (CCR), is eliminated.

The FLC technique has been used in the context of power electronics, for example to control ac-dc rectifiers [19], [20], modular multilevel converters [21] and synchronous motor drives [22]. Use of the FLC technique is documented in [23]–[25] for output voltage controlled dc-dc converters, albeit without hardware implementation or experimental results. In the context of PV systems, the FLC technique has been mostly studied to control single-stage grid-connected PV inverters. In [26]–[28] and [29], the input voltage and the power factor of a three-phase PV inverter, connected to the utility grid via an inductive filter, are controlled by applying the FLC technique. The same control objectives are achieved in [30], where the FLC technique is applied to a more complex configuration, entailing the grid connection of the PV inverter via a *LCL* filter, as opposed to a simple inductive filter. Although [26]–[30] enrich the literature on FLC in PV systems, they concern control of three-phase inverters, rather than PV interfacing dc-dc converters. Recently, [31] discussed the application of the FLC technique to regulate the input voltage of a PV interfacing boost converter. Nonetheless, [31] uses a single-loop voltage control scheme, as opposed to a cascaded control scheme, which is analyzed in this paper. Moreover, among [26]–[31], only [28], [30] and [31] present an experimental validation. There clearly exists a gap in the technical literature, where the FLC technique, with a cascaded loop structure, has not been applied to control the PV interfacing non-inverting buck-boost converter. This knowledge gap is addressed by this article, whose contribution lies in the application of the FLC technique in the non-inverting buck-boost topology, which was not studied in the existing literature, with the provision of experimental evidence.

In the next section, the linear cascaded control approach based on small-signal transfer functions is reviewed, with special attention to the issue of the converter operation in the buck mode, while the PV source is in the CCR. In Section III, the input/output feedback linearization framework is applied to design a non-linear controller for the selected dc-MIC. A 200 W non-inverting buck-boost dc-MIC prototype switched at 200 kHz, and a digital control platform based on a Texas Instruments TMS320F28377D floating point microcontroller, have been designed and built. This system is used in Section IV to draw experimental results, where the PV module voltage regulation is analyzed. Firstly, it is shown that the FLC scheme, although is entailing the control of the average inductor current, is not subjected to stability issues, when PV source operates in the CCR and the converter works in the buck mode. Secondly, a close comparison between the transient performance of the converter controlled with the FLC technique vs. the linear cascaded control technique is included in the experimental results, followed by the Conclusion in Section V.

II. Issues with Linear Cascaded Controller

Prior to discussing the FLC technique, it is opportune to highlight the limitations of the PV interfacing buck-boost dc-MIC under the linear cascaded control scheme. In order to do so, it is necessary to review some important properties of the PV generator and the converter small-signal transfer functions.

A. Properties of the PV Generator

Letting the PV module in Fig. 1 be represented by the well-known five-parameter equivalent circuit [32], then the PV current, $i_{\rm pv}$, is given by:

$$i_{\rm pv} = I_{\rm ph} - I_{\rm o}\left(e^{\frac{v_{\rm pv}+R_{\rm s}i_{\rm pv}}{nN_{\rm s}V_{\rm th}}} - 1\right) - \frac{v_{\rm pv}+R_{\rm s}i_{\rm pv}}{R_{\rm p}} \quad (1)$$

with $I_{\rm ph}$ the photo-generated current, proportional to the received solar irradiation, $I_{\rm o}$ the diode-dark saturation current, n the diode ideality factor, $R_{\rm s}$ and $R_{\rm p}$ the series resistance and shunt resistance, respectively, $N_{\rm s}$ the number of series connected PV cells forming the PV module, n is the diode ideality factor, and $V_{\rm th}$ the thermal voltage [32]. As illustrated in Fig. 2a, valid for a sample PV module having an MPP voltage of $V_{\rm mpp}$ = 26 V, the relationship between PV voltage, $v_{\rm pv}$, and current, $i_{\rm pv}$, given by (1) is highly non-linear. In the proximity of a quiescent point having coordinate ($V_{\rm pv}$, $I_{\rm pv}$), the non-linear *i-v* curve in Fig. 2a can be approximated by its tangent, whose equation is characteristic of a Thevenin equivalent circuit [15], and it is given by:

$$v_{\rm pv} = E - r_{\rm pv}i_{\rm pv} \quad (2)$$

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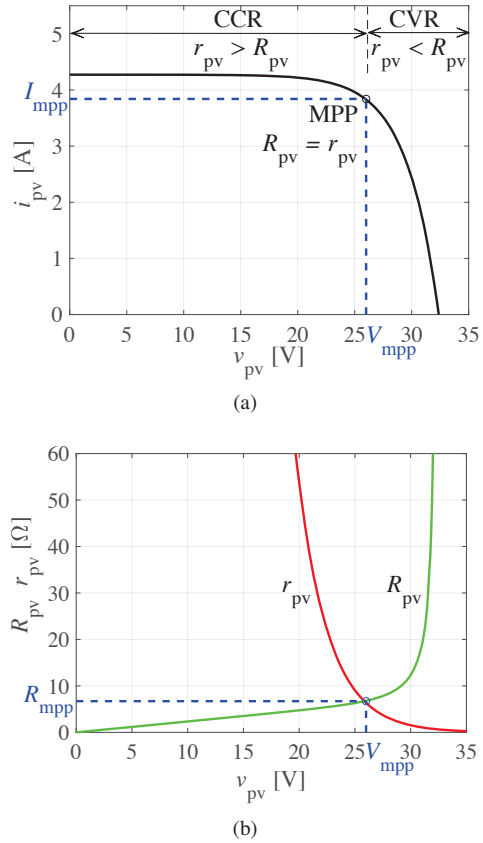

Fig. 2. Characteristic curves of the PV module (at constant solar irradiation and temperature). (a) Operating regions in the *i-v* curve. (b) Dynamic and static resistance curves.

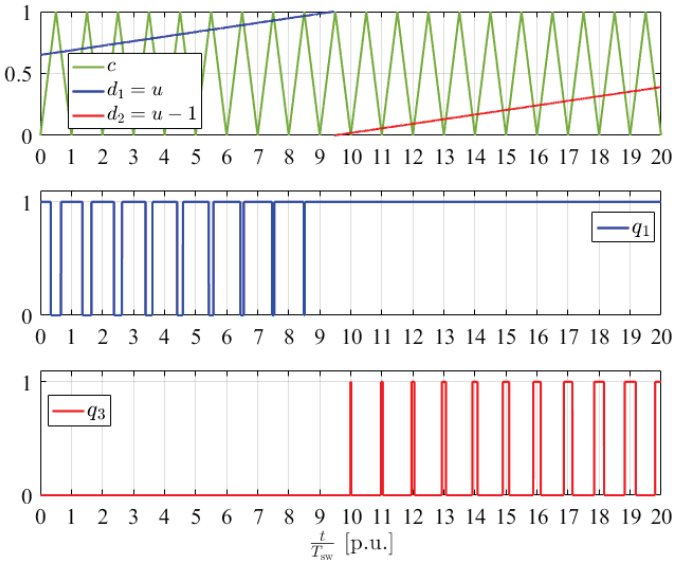

Fig. 3. Modulation technique for the dc-MIC in Fig. 1. (Top) PWM carrier, buck and boost control signals. (Middle) Buck leg PWM_1, q_2 is complementary to q_1. (Bottom) Boost leg PWM_2, q_4 is complementary to q_3.

TABLE I
NON-INVERTING BUCK-BOOST DC-MIC OPERATING MODE SUMMARY

Operation Mode	S1	S2	S3	S4
Buck	$d_1 > 0$	$1 - d_1 > 0$	$d_2 = 0$	$1 - d_2 = 1$
Boost	$d_1 = 1$	$1 - d_1 = 0$	$d_2 > 0$	$1 - d_2 > 0$
Buck-Boost or Pass-through	$d_1 > 0$ $d_1 = 1$	$1 - d_1 > 0$ $1 - d_1 = 0$	$d_2 > 0$ $d_2 = 0$	$1 - d_2 > 0$ $1 - d_2 = 1$

where the Thevenin equivalent voltage source and series resistance are respectively:

$$E = (r_{\rm pv} I_{\rm pv} + V_{\rm pv}) \tag{3}$$

$$r_{\rm pv} = -\left.\frac{\partial v_{\rm pv}}{\partial i_{\rm pv}}\right|_{\substack{v_{\rm pv}=V_{\rm pv}\\ i_{\rm pv}=I_{\rm pv}}} = -\frac{\tilde{v}_{\rm pv}}{\tilde{i}_{\rm pv}} \tag{4}$$

Eq. (4) represents the PV source *dynamic resistance*, it is a positive quantity [10], and it can be written in terms of the small-signal variation of the PV module voltage, $\tilde{v}_{\rm pv}$, and current, $\tilde{i}_{\rm pv}$, from the quiescent point ($V_{\rm pv}$, $I_{\rm pv}$).

For a generic quiescent point, the PV source *static resistance* is defined as:

$$R_{\rm pv} \triangleq \frac{V_{\rm pv}}{I_{\rm pv}} \tag{5}$$

allowing to further classify the behavior of the PV source, depending on the quiescent point location in the *i-v* curve. The graph in Fig. 2b displays the behavior of (4) and (5), related to the *i-v* curve in Fig. 2a. Observing Fig. 2a and 2b, the constant current region (CCR) is defined as the zone on the left of the MPP, where the dynamic resistance is greater than the static resitance, $r_{\rm pv} > R_{\rm pv}$; at the MPP, dynamic and static resistance are equal [33], $r_{\rm pv} = R_{\rm pv}$; finally in the constant voltage region (CVR) the dynamic resistance is smaller than the static resistance, $r_{\rm pv} < R_{\rm pv}$ [10].

B. Interfacing Converter Small-Signal Analysis

Before discussing the small-signal analysis, the non-inverting buck-boost dc-MIC operation is briefly reviewed. This converter, shown Fig. 1, operates either in buck mode or in boost mode; each control switch (S_1, S_3) has a respective synchronous rectifier (S_2, S_4) [34, p. 73]. In the buck mode, the buck leg switches are operated according to the duty cycle d_1 of the buck-control switch S_1, while the boost-control switch S_3 is permanently off. In the boost mode, S_1 is always on, while the duty cycle d_2 of the boost leg control switch, S_3, determines the boost operation. These modes of operation are illustrated in Fig. 3. Whenever the output voltage $v_{\rm o}$ approaches the input voltage $v_{\rm pv}$, the converter is required to operate at a voltage conversion ratio close to one, which may not be achievable with the buck or boost operation alone. In such instance, either a special buck-boost mode [35] or a pass-through mode [36] is applied. In the first case, both legs are switched simultaneously in every switching cycle, while in the second case, S_1 and S_4 are constantly turned-on, with S_2 and S_3 constantly turned-off. This paper refers to the individual buck or boost regime, leaving the combined buck-boost or the pass-through modes to the above-mentioned literature. A summary of the converter operating modes is reported in Table I.

The duty cycle d_1 and d_2 are the control inputs to the converter. The switching cycle averaged state equations for

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the circuit in Fig. 1 are:

$$\frac{dv_{\rm pv}}{dt} = \frac{i_{\rm pv}}{C_{\rm i}} - \frac{d_1 i_{\rm L}}{C_{\rm i}} \tag{6}$$

$$\frac{di_{\rm L}}{dt} = \frac{d_1 v_{\rm pv}}{L} - \frac{R_{\rm L} i_{\rm L}}{L} - \frac{(1-d_2)v_{\rm o}}{L} \tag{7}$$

where $i_{\rm L}$ and $v_{\rm pv}$ are the state variables. The converter output voltage is not a state variable and is assumed to be constant. In fact, as seen in [5, eq. (22)], $v_{\rm o}$ depends on the PV power, whose rate of change is very slow compared to the bandwidth of the PV module voltage control loop [37]. Following perturbation and linearization of (6) and (7) about a quiescent point, the linear small-signal state equations can be written in the state-space form $\frac{d\tilde{\mathbf{x}}}{dt} = \mathbf{A}\tilde{\mathbf{x}} + \mathbf{B}\tilde{\mathbf{u}}$:

$$\begin{bmatrix} \frac{d\tilde{v_{\rm pv}}}{dt} \\ \frac{d\tilde{i_{\rm L}}}{dt} \end{bmatrix} = \begin{bmatrix} \frac{-1}{r_{\rm pv}C_{\rm i}} & \frac{-D_1}{C_{\rm i}} \\ \frac{D_1}{L} & \frac{-R_{\rm L}}{L} \end{bmatrix} \begin{bmatrix} \tilde{v_{\rm pv}} \\ \tilde{i_{\rm L}} \end{bmatrix} + \begin{bmatrix} \frac{-I_{\rm L}}{C_{\rm i}} & 0 & 0 \\ \frac{V_{\rm pv}}{L} & \frac{V_{\rm o}}{L} & \frac{D_2-1}{L} \end{bmatrix} \begin{bmatrix} \tilde{d_1} \\ \tilde{d_2} \\ \tilde{v_{\rm o}} \end{bmatrix} \tag{8}$$

where the values inside the matrices $\mathbf{A}$ and $\mathbf{B}$ pertain to the quiescent point, the small-signal state variables are represented by $\tilde{\mathbf{x}} = [\tilde{v}_{\rm pv}\ \tilde{i}_L]^T$, and the small-signal inputs are represented by $\tilde{\mathbf{u}} = [\tilde{d_1}\ \ \tilde{d_2}\ \ \tilde{v}_o]^T$. Choosing the small-signal outputs to be represented by $\tilde{\mathbf{y}} = [\tilde{v}_{\rm pv}\ \tilde{i}_L]^T$ and by virtue of the Laplace transform, the linear relation between each small-signal input and output can be found using the well-known formula $\tilde{\mathbf{y}}(s) = [(s\mathbf{I} - \mathbf{A})^{-1}\mathbf{B}]\tilde{\mathbf{u}}(s)$, where $\mathbf{I}$ is a 2×2 identity matrix, yielding:

$$\begin{bmatrix} \tilde{v}_{\rm pv}(s) \\ \tilde{i}_{\rm L}(s) \end{bmatrix} = \begin{bmatrix} G_{v_{\rm pv}d_1} & G_{v_{\rm pv}d_2} & G_{v_{\rm pv}v_{\rm o}} \\ G_{i_{\rm L}d_1} & G_{i_{\rm L}d_2} & G_{i_{\rm L}v_{\rm o}} \end{bmatrix} \begin{bmatrix} \tilde{d_1}(s) \\ \tilde{d_2}(s) \\ \tilde{v}_{\rm o}(s) \end{bmatrix} \tag{9}$$

From (9), the duty cycle-to-PV module voltage and the duty cycle-to-inductor current plant transfer functions, used for the linear cascaded controller design, are:

$$G_{v_{\rm pv}d_1} = \frac{\tilde{v}_{\rm pv}}{\tilde{d}_1} = -\frac{r_{\rm pv}\left(\frac{D_1V_{\rm pv}+R_{\rm L}I_{\rm L}}{D_1^2r_{\rm pv}+R_{\rm L}}\right)\left(s\frac{I_{\rm L}L}{D_1V_{\rm pv}+R_{\rm L}I_{\rm L}}+1\right)}{s^2\left(\frac{r_{\rm pv}LC_{\rm i}}{D_1^2r_{\rm pv}+R_{\rm L}}\right)+s\left(\frac{C_{\rm i}R_{\rm L}r_{\rm pv}+L}{D_1^2r_{\rm pv}+R_{\rm L}}\right)+1} \tag{10}$$

$$G_{v_{\rm pv}d_2} = \frac{\tilde{v}_{\rm pv}}{\tilde{d}_2} = -\frac{\left(\frac{D_1r_{\rm pv}V_{\rm o}}{D_1^2r_{\rm pv}+R_{\rm L}}\right)}{s^2\left(\frac{r_{\rm pv}LC_{\rm i}}{D_1^2r_{\rm pv}+R_{\rm L}}\right)+s\left(\frac{C_{\rm i}R_{\rm L}r_{\rm pv}+L}{D_1^2r_{\rm pv}+R_{\rm L}}\right)+1} \tag{11}$$

$$G_{i_{\rm L}d_1} = \frac{\tilde{i}_{\rm L}}{\tilde{d}_1} = \frac{\left(\frac{V_{\rm pv}-D_1I_{\rm L}r_{\rm pv}}{D_1^2r_{\rm pv}+R_{\rm L}}\right)\left(s\frac{C_{\rm i}r_{\rm pv}V_{\rm pv}}{V_{\rm pv}-D_1I_{\rm L}r_{\rm pv}}+1\right)}{s^2\left(\frac{r_{\rm pv}LC_{\rm i}}{D_1^2r_{\rm pv}+R_{\rm L}}\right)+s\left(\frac{C_{\rm i}R_{\rm L}r_{\rm pv}+L}{D_1^2r_{\rm pv}+R_{\rm L}}\right)+1} \tag{12}$$

$$G_{i_{\rm L}d_2} = \frac{\tilde{i}_{\rm L}}{\tilde{d}_2} = \frac{\left(\frac{V_{\rm o}}{D_1^2r_{\rm pv}+R_{\rm L}}\right)(sC_{\rm i}r_{\rm pv}+1)}{s^2\left(\frac{r_{\rm pv}LC_{\rm i}}{D_1^2r_{\rm pv}+R_{\rm L}}\right)+s\left(\frac{C_{\rm i}R_{\rm L}r_{\rm pv}+L}{D_1^2r_{\rm pv}+R_{\rm L}}\right)+1} \tag{13}$$

where the subscript 1 refers to the buck mode of operation, while the subscript 2 to the boost mode. Eq. (10) and (12) assume $\tilde{d}_2 = 0$ and $\tilde{v}_{\rm o} = 0$, while (11) and (13) assume $\tilde{d}_1 = 0$ and $\tilde{v}_{\rm o} = 0$. The inductor current-to-PV module voltage transfer functions, needed for the design of the PV module voltage controller can be found utilizing (10)-(13) and these are:

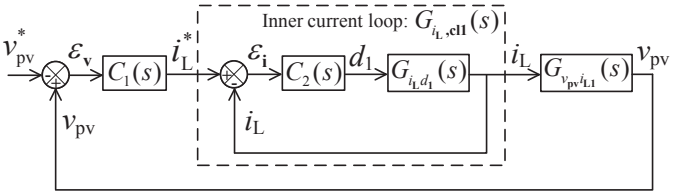

Fig. 4. Linear cascaded controller. The inner loop regulates the average inductor current, the outer loop regulates the PV module voltage.

$$G_{v_{\rm pv}i_{\rm L_1}} = \frac{\frac{\tilde{v}_{\rm pv}}{\tilde{d}_1}}{\frac{\tilde{i}_{\rm L}}{\tilde{d}_1}} = -\frac{r_{\rm pv}\left(\frac{D_1V_{\rm pv}+R_{\rm L}I_{\rm L}}{V_{\rm pv}-D_1I_{\rm L}r_{\rm pv}}\right)\left(s\frac{I_{\rm L}L}{D_1V_{\rm pv}+R_{\rm L}I_{\rm L}}+1\right)}{\left(s\frac{C_{\rm i}r_{\rm pv}V_{\rm pv}}{V_{\rm pv}-D_1I_{\rm L}r_{\rm pv}}+1\right)} \tag{14}$$

$$G_{v_{\rm pv}i_{\rm L_2}} = \frac{\frac{\tilde{v}_{\rm pv}}{\tilde{d}_2}}{\frac{\tilde{i}_{\rm L}}{\tilde{d}_2}} = -\frac{r_{\rm pv}D_1}{(sC_{\rm i}r_{\rm pv}+1)} \tag{15}$$

for the buck and the boost operating mode, respectively.

C. Buck Mode Instability with Linear Cascaded Controller

In the traditional linear cascaded control scheme, a fast inner loop regulates the average inductor current, while a slower outer loop regulates the PV module voltage. The linear cascaded control diagram is shown in Fig. 4, for the buck mode. Stability becomes a concern when designing the outer loop controller $C_1(s)$. In fact, with the inner loop bandwidth much greater than the outer loop bandwidth, from the perspective of the outer voltage loop, the inner closed-loop is infinitely fast, reaching instantly $i_{\rm L}^* = i_{\rm L}$, with $G_{\rm i_{L,\,cl1}}(s) = \frac{\tilde{i}_{\rm L}}{\tilde{i}_{\rm L}^*} = 1$. Therefore, the plant transfer function for the design of the outer loop controller is simply $G_{v_{\rm pv}i_{\rm L_1}}(s)$, given in (14). This transfer function has one pole in $s = -\omega_{\rm p1}$, where $\omega_{\rm p1}$ is equal to:

$$\omega_{\rm p1} = \frac{V_{\rm pv} - D_1I_{\rm L}r_{\rm pv}}{C_{\rm i}r_{\rm pv}V_{\rm pv}} \tag{16}$$

In the buck mode, disregarding losses for simplicity, the converter dc input current can be expressed as $I_{\rm pv} = D_1I_{\rm L}$, therefore, collecting $I_{\rm pv}$ and using (5) allows writing the numerator of (16) as $I_{\rm pv}\,(R_{\rm pv} - r_{\rm pv})$. It follows that the instability condition $\omega_{\rm p1} < 0$ (the pole is in the right half of the complex plane) occurs when:

$$r_{\rm pv} > R_{\rm pv} \tag{17}$$

In other words the plant $G_{v_{\rm pv}i_{\rm L_1}}(s)$, in Fig 4, is unstable when the PV source quiescent point is in the CCR (Fig. 2a).

Since the dc-MIC is operated in the closed-loop, the eventual instability condition needs to be analyzed when the controller $C_1(s)$ is in the loop. Assuming that a proportional integral (PI) controller is adopted, it is:

$$C_1(s) = k_{\rm p1} + \frac{k_{\rm i1}}{s} \tag{18}$$

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and the closed-loop transfer function for the outer voltage loop, under the stated assumption of a fast current loop, is:

$$G_{\mathrm{v_{pv},cl1}}(s) = \frac{\tilde{v}_{\mathrm{pv}}}{\tilde{v}^{*}_{\mathrm{pv}}} = \frac{-C_1(s)G_{v_{\mathrm{pv}}i_{\mathrm{L}1}}(s)}{1 - C_1(s)G_{v_{\mathrm{pv}}i_{\mathrm{L}1}}(s)} \tag{19}$$

The stability of the closed-loop PV voltage regulation system can be ensured by analyzing the denominator of (19), and verifying that none of its poles lie in the right half of the complex plane. In (19), the term $G_{v_{\mathrm{pv}}i_{\mathrm{L}1}}(s)$ can be expressed in the convenient form:

$$G_{v_{\mathrm{pv}}i_{\mathrm{L}1}}(s) = K_1\frac{(s+\omega_{\mathrm{z1}})}{(s+\omega_{\mathrm{p1}})} \tag{20}$$

where ω_{p1} is from (16), while ω_{z1} and K_1 are respectively:

$$\omega_{\mathrm{z1}} = \frac{D_1V_{\mathrm{pv}} + R_{\mathrm{L}}I_{\mathrm{L}}}{I_{\mathrm{L}}L} \tag{21}$$

$$K_1 = -\frac{I_{\mathrm{L}}L}{C_{\mathrm{i}}V_{\mathrm{pv}}} \tag{22}$$

Using (18) and (20) inside of (19), allows to find an expression for the denominator of (19), $D(s)$, in the polynomial form:

$$D(s) = s^2(1-K_1k_{\mathrm{p1}}) + s(\omega_{\mathrm{p1}} - K_1k_{\mathrm{i1}} - K_1k_{\mathrm{p1}}\omega_{\mathrm{z1}}) - K_1k_{\mathrm{i1}}\omega_{\mathrm{z1}} \tag{23}$$

The roots of (23) are in the left half of the complex plane, and the closed-loop system (19) is stable, as long as (23) is a Hurwitz polynomial, i.e. all its coefficients are real and positive. Using (21) and (22), the coefficient of the s^0 term of (23) is:

$$-K_1k_{\mathrm{i1}}\omega_{\mathrm{z1}} = -\left(-\frac{I_{\mathrm{L}}L}{C_{\mathrm{i}}V_{\mathrm{pv}}}\right)k_{\mathrm{i1}}\left(\frac{D_1V_{\mathrm{pv}} + R_{\mathrm{L}}I_{\mathrm{L}}}{I_{\mathrm{L}}L}\right) \tag{24}$$

and it is always greater than zero, since all its coefficients are positive. The coefficient of the s^2 term of (23) is:

$$1 - K_1k_{\mathrm{p1}} = 1 + \frac{I_{\mathrm{L}}L}{C_{\mathrm{i}}V_{\mathrm{pv}}}k_{\mathrm{p1}} \tag{25}$$

being greater than zero if

$$k_{\mathrm{p1}} > -\left(\frac{C_{\mathrm{i}}V_{\mathrm{pv}}}{I_{\mathrm{L}}L}\right) \tag{26}$$

which is always satisfied, because k_{p1} is a positive number. The last condition to ensure the absence of closed-loop poles in the right half plane is to have the coefficient of the s^1 term of (23) greater than zero, which translates to the condition:

$$\omega_{\mathrm{p1}} - K_1k_{\mathrm{i1}} - K_1k_{\mathrm{p1}}\omega_{\mathrm{z1}} = \frac{V_{\mathrm{pv}} - D_1I_{\mathrm{L}}r_{\mathrm{pv}}}{r_{\mathrm{pv}}} + k_{\mathrm{i1}}I_{\mathrm{L}}L + k_{\mathrm{p1}}\left(D_1V_{\mathrm{pv}} + R_{\mathrm{L}}I_{\mathrm{L}}\right) > 0 \tag{27}$$

Disregarding the inductance series resistance, $R_{\mathrm{L}} \approx 0$, considering $k_{\mathrm{i}}I_{\mathrm{L}}L << k_{\mathrm{p1}}D_1V_{\mathrm{pv}}$ and reminding that in the buck mode $D_1V_{\mathrm{pv}} = V_{\mathrm{o}}$, after some algebra (27) yields:

$$k_{\mathrm{p1}} > \frac{I_{\mathrm{pv}}\left(r_{\mathrm{pv}} - R_{\mathrm{pv}}\right)}{r_{\mathrm{pv}}V_{\mathrm{o}}} \tag{28}$$

which is the the only condition to satisfy in order to ensure the stability of the closed-loop system, in the buck mode, since k_{p1} and k_{i1} are positive. In summary, so far it has been demonstrated that with the linear cascaded control scheme of Fig. 4, the proportional gain of the outer voltage loop PI controller must satisfy (28) to ensure the closed-loop system stability, when the converter is operating in the buck mode. The right-hand side term of (28) is negative in the CVR, or is zero at the MPP, hence in these instances (28) is always satisfied, since k_{p1} is a positive quantity. In the CCR, where $r_{\mathrm{pv}} > R_{\mathrm{pv}}$, the term on the right-hand side of (28) is positive, therefore highlighting a potential stability issue if k_{p1} is not large enough.

Among several literary resources, [14]–[16], [38] propose strategies to choose a value of the outer loop controller proportional gain, k_{p1}, which is large enough to avoid closed-loop instability issues. However, should k_{p1} unexpectedly change for reasons beyond the designer's influence, condition (28) may be violated, with detrimental impact on the closed-loop stability. In other words, the system is not robust, as large changes in the value of the outer loop controller k_{p1}, can jeopardize the stability, even if this was initially ensured by the fulfillment of (28).

Although both the PV module voltage and the average inductor current are controlled with the feedback linearization scheme proposed in the next section, the stability issue affecting the converter, and articulated thus far, is avoided. With feedback linearization, the closed-loop stability is not threatened by large changes in the value of the outer loop controller proportional gain, considerably improving the robustness of the system.

III. Feedback Linearization Control Framework

Before analyzing benefits of the FLC technique in comparison with the linear cascaded controller, the FLC laws are derived starting from the switching cycle averaged state equations (6) and (7). The non-linearity in (6) and (7) is due to the cross-product between the converter control inputs (d_1 and d_2) and the state variables (v_{pv} and i_{L}), and by the presence of the non-linear term i_{pv}, which varies according to (1). In the following paragraphs, a non-linear cascaded controller is designed by means of the input/output FLC technique. Thanks to this technique, the non-linearities in the average equations (6) and (7) are eliminated by appropriate selection of new control inputs.

A. Boost Mode Feedback Linearization Control Law

The following analysis of the boost mode is made by posing d_1 = 1 in (6) and (7), and neglecting the voltage drop $R_{\mathrm{L}}i_{\mathrm{L}}$, for the sake of simplicity. The inner loop regulates the average value of the inductor current, i_{L}. The inductor current dynamic equation (7), where i_{L} is the state variable chosen as output, and d_2 is the control input, can be transformed into a linear equation if v_{L} is taken as the new control input for the current loop (rather than d_2). The inductor current dynamics can therefore be expressed by means of the linear equation:

$$\frac{di_{\mathrm{L}}}{dt} = \frac{v_{\mathrm{L}}}{L} \tag{29}$$

A linear current controller $G_{\mathrm{ci}}(s)$, whose output is v_{L} , can be designed based on the analysis of (29), noting that the

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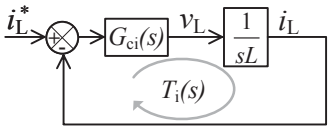

Fig. 5. Block diagram for designing the current controller $G_{\mathrm{ci}}(s)$. The new linear plant described by (29) is between v_{L} and i_{L}. $T_{\mathrm{i}}(s)$ is the open-loop transfer function, for the inner current loop.

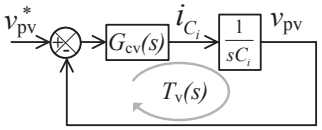

Fig. 6. Block diagram for designing the voltage controller $G_{\mathrm{cv}}(s)$. The new linear plant described by (34) is between $i_{\mathrm{C_i}}$ and v_{pv}. $T_{\mathrm{v}}(s)$ is the open-loop transfer function for the displayed outer voltage loop.

transfer function from the new control input, v_{L}, to the output, i_{L}, is simply given by $\frac{1}{sL}$ (Fig. 5). If a proportional integral (PI) current controller is chosen, then substituting v_{L} with an expression including the controller parameters, turns (29) into:

$$\frac{di_{\mathrm{L}}}{dt} = \frac{1}{L}\left[k_{\mathrm{p_i}}\left(i_{\mathrm{L}}^* - i_{\mathrm{L}}\right) + k_{\mathrm{ii}}\xi_{\mathrm{i}}\right] \tag{30}$$

$$\frac{d\xi_{\mathrm{i}}}{dt} = i_{\mathrm{L}}^* - i_{\mathrm{L}} \tag{31}$$

in which ξ_{i} is the integrator output. Using v_{L} as the new control input allowed to design $G_{\mathrm{ci}}(s)$ around a simple plant transfer function, given by $\frac{1}{sL}$. However, the actual control input to the converter in boost mode is d_2, and an expression for it must be derived. If (30) is substituted into (7), d_2 results:

$$d_2|_{d_1=1} = 1 - \frac{v_{\mathrm{pv}} - \left[k_{\mathrm{p_i}}\left(i_{\mathrm{L}}^* - i_{\mathrm{L}}\right) + k_{\mathrm{ii}}\xi_{\mathrm{i}}\right]}{v_{\mathrm{o}}} \tag{32}$$

which is the sought *inner current loop control law for the boost mode*.

The outer voltage loop regulates the PV module voltage and provides the reference, i_{L}^*, to the inner current control loop. As the outer loop is slower than the inner loop, when analyzing the former, the simplifying assumption $i_{\mathrm{L}}^* \cong i_{\mathrm{L}}$ is made. Therefore, from the outer voltage loop perspective, the dynamics of the inductor current can be disregarded. In fact, with $i_{\mathrm{L}}^* \cong i_{\mathrm{L}}$, (32) yields $1 - d_2 \cong \frac{v_{\mathrm{pv}}}{v_{\mathrm{o}}}$, which substituted in (7) returns $\frac{di_{\mathrm{L}}}{dt} \cong 0$, as expected. Thanks to the fast current control, the PV module voltage dynamics is redefined by:

$$C_{\mathrm{i}}\frac{dv_{\mathrm{pv}}}{dt} \cong i_{\mathrm{pv}} - i_{\mathrm{L}}^* \tag{33}$$

in which i_{L}^* is the outer voltage loop control input and v_{pv} the state variable, chosen as output. The non-linearity in (33) is due to the presence of the PV module current i_{pv}, in fact $i_{\mathrm{pv}} = f\left(i_{\mathrm{pv}}, v_{\mathrm{pv}}\right)$. Choosing $i_{\mathrm{C_i}}$ as the new control input for the voltage loop (rather than i_{L}^*), yields to the linear expression for the PV module voltage dynamics:

$$\frac{dv_{\mathrm{pv}}}{dt} = \frac{i_{\mathrm{C_i}}}{C_{\mathrm{i}}} \tag{34}$$

Based on (34), the transfer function from $i_{\mathrm{C_i}}$ to v_{pv} is simply given by $\frac{1}{sC_{\mathrm{i}}}$ (Fig. 6), therefore a linear voltage controller $G_{\mathrm{cv}}(s)$, whose output is $i_{\mathrm{C_i}}$, can be easily designed. If $G_{\mathrm{cv}}(s)$ is carried out by means of a PI controller, eliciting the controller parameters, turns (34) into:

$$\frac{dv_{\mathrm{pv}}}{dt} = \frac{1}{C_{\mathrm{i}}}\left[k_{\mathrm{pv}}(v_{\mathrm{pv}}^* - v_{\mathrm{pv}}) + k_{\mathrm{iv}}\xi_{\mathrm{v}}\right] \tag{35}$$

$$\frac{d\xi_v}{dt} = v_{\mathrm{pv}}^* - v_{\mathrm{pv}} \tag{36}$$

in which ξ_{v} is the integrator output. In the same manner that was used to derive the actual control input for the inner current loop, d_2, an expression for the actual control input of the outer voltage loop, i_{L}^*, must be derived. Using (35) inside of (33), gives:

$$i_{\mathrm{L}}^*|_{d_1=1} = i_{\mathrm{pv}} - k_{\mathrm{p_v}}(v_{\mathrm{pv}}^* - v_{\mathrm{pv}}) - k_{\mathrm{iv}}\xi_{\mathrm{v}} \tag{37}$$

which is the sought *outer voltage loop control law for the boost mode*. Since for the outer loop it is $i_{\mathrm{L}}^* \cong i_{\mathrm{L}}$, substitution of (37) into (33), cancels the non-linearity caused by i_{pv}. In summary, the non-linear cascaded controller for the boost mode designed with the FLC technique, is represented by (32), governing the inner current loop, together with (37), governing the outer voltage loop.

B. Buck Mode Feedback Linearization Control Laws

For the dc-MIC operation in buck mode, $d_2 = 0$ in (6) and (7); furthermore the voltage drop $R_L i_L$ is again neglected for simplicity. In the same fashion of Section III-A, the *control law of the inner current loop for the buck mode* is derived as:

$$d_1|_{d_2=0} = \frac{v_{\mathrm{o}} + \left[k_{\mathrm{p_i}}\left(i_{\mathrm{L}}^* - i_{\mathrm{L}}\right) + k_{\mathrm{ii}}\xi_{\mathrm{i}}\right]}{v_{\mathrm{pv}}} \tag{38}$$

with ξ_{i} conforming to (31).

The outer voltage loop is again studied considering an inner current loop faster that the outer voltage loop, so that from the perspective of the latter it is $i_L^* \cong i_L$, i.e. the inductor current dynamic is neglected. In the strength of this assumption, for the outer voltage loop in the buck mode, (38) yields $d_1 \cong \frac{v_o}{v_{\mathrm{pv}}}$. When this is substituted into (7), it results in $\frac{di_L}{dt} \cong 0$, as anticipated. Based on these assumptions, using the linear equation (34) for the PV module voltage dynamics, the *control law of the outer voltage loop in the buck mode* can be derived from (6), returning:

$$i_{\mathrm{L}}^*|_{d_2=0} = \frac{v_{\mathrm{pv}}}{v_{\mathrm{o}}}\left\{i_{\mathrm{pv}} - \left[k_{\mathrm{p_v}}(v_{\mathrm{pv}}^* - v_{\mathrm{pv}}) + k_{\mathrm{iv}}\xi_{\mathrm{v}}\right]\right\} \tag{39}$$

with ξ_{v} obeying to (36). The designed cascaded control loop for the buck mode, is represented by (38), governing the inner current loop, together with (39), governing the outer voltage loop. The integrator laws, (31) and (36), are the same as for the boost mode.

C. Feedback Linearization Controller Design

A unified non-linear cascaded controller, suitable for the buck and the boost operation, is now designed based upon the control laws derived in the previous section. While the

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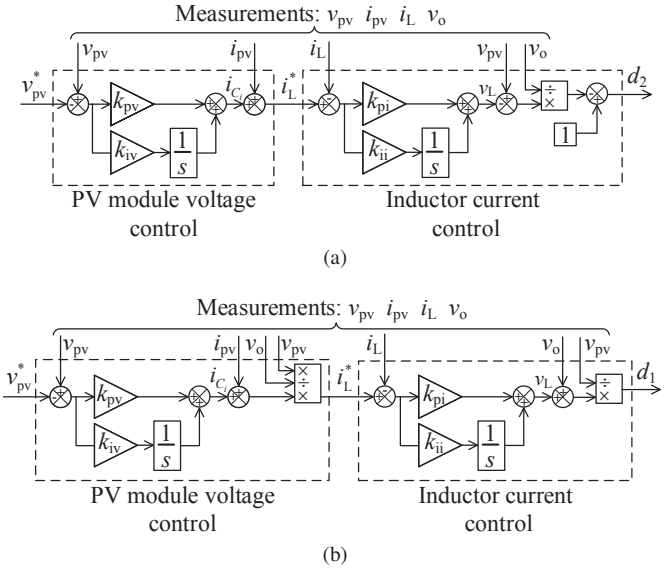


Fig. 7. Controller designed with the proposed technique. (a) Control scheme for boost operation ($d_1 = 1$). (b) Control scheme for buck operation ($d_2 = 0$).

PI controllers $G_{cv}(s)$ and $G_{ci}(s)$ remain the same for either the buck or the boost operation, the measured variables are employed either according to the control laws (32) and (37), for the boost mode (Fig. 7a), or conforming to (38) and (39), for the buck mode (Fig. 7b). The inner loop PI controller, $G_{ci}(s)$, is determined based on the analysis of Fig. 5, derived from (29), which holds for both the buck and the boost operating modes. In principle, a simple proportional (P) controller would be adequate to achieve the desired regulation, as the plant transfer function ($\frac{1}{sL}$) contains in itself an integrator. In practice though, parasitic resistances should be accounted for in the plant transfer function, having the effect of reducing the system gain at low frequencies, therefore causing a small steady-state error. For this reason $G_{ci}(s)$ and $G_{cv}(s)$ include a small integral part, so that steady-state errors due to parasitic resistances in the plant transfer function can be eliminated.

With attention to Fig. 5 for the inductor current loop, the open-loop transfer function is simply given by:

$$T_i(s) = \frac{G_{ci}(s)}{sL} \tag{40}$$

The the PI controller is expressed as:

$$G_{ci}(s) = k_{pi} + \frac{k_{ii}}{s} = \frac{k_{ii}}{s}\left(s\frac{k_{pi}}{k_{ii}} + 1\right) \tag{41}$$

highlighting the pole at the origin and the zero at the angular frequency $\omega_{zi} = k_{ii}/k_{pi}$. The speed of the inner current loop relates to its open-loop transfer function $T_i(s)$ cross-over frequency [39, p. 288], $\omega_i = 2\pi f_i$, at which $|T_i(j\omega_i)| = 1$. If $0 \ll f_i \ll f_{sw}$, with f_{sw} the converter switching frequency, then at ω_i it is $G_{ci}(s) \approx k_{pi}$. Evaluating (40) at ω_i gives:

$$|T_i(j\omega_i)| = 1 \approx \frac{k_{pi}}{\omega_i L} \tag{42}$$

from which k_{pi} is chosen as $k_{pi} = 2\pi f_i L$. The integrator gain, k_{ii}, is found imposing that the zero at ω_{zi} in $G_{ci}(s)$ is far removed from the cross-over frequency ω_i. It is chosen:

$$\frac{k_{ii}}{k_{pi}} = 10^{-3}\omega_i, \tag{43}$$

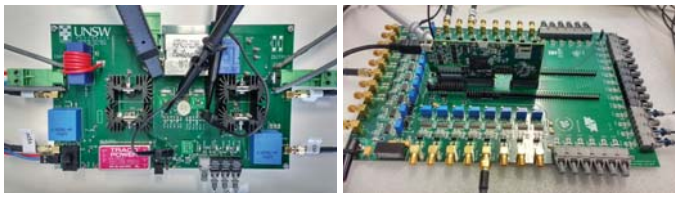
resulting in $k_{ii} = 10^{-3}\omega_i k_{pi}$. In a similar fashion, the gains k_{pv} and k_{iv} for the outer loop controller $G_{cv}(s)$ can be calculated. As the aim is to have an outer voltage loop slower than the inner current loop, the cross-over frequency of the outer loop, named ω_v, is chosen to be significantly smaller than the cross-over frequency of the inner current loop, ω_i, such that $\omega_v = 0.1\omega_i$ or $0.2\omega_i$. The gains k_{pv} and k_{iv} are elicited adopting the same framework used to derive k_{pi} and k_{ii}. This time the reference is made to Fig. 6, where the plant transfer function has been derived by applying the Laplace transform to (34). The open-loop transfer function is in this case:

$$T_v(s) = \frac{G_{cv}(s)}{sC_i} \tag{44}$$

Finally, it is $k_{pv} = \omega_v C_i$ and $k_{iv} = 10^{-3}\omega_v k_{pv}$.

TABLE II
CONVERTER AND MICROCONTROLLER KEY PARAMETERS

Converter	Value	Notes
Inductance	L = 22 μH	Coilcraft AGP4233 [40]
Inductance series resistance	R_L = 20 mΩ	
Input capacitance	C_i = 110 μF	Ceramic capacitors
Output capacitance	C_o = 2.4 μF	Ceramic capacitors
Switching frequency	f_{sw} = 200 kHz	T_{sw} = 5 μs
MOSFETs	I/V ratings 100 A/150 V	Silicon, Infineon IPP075N15N3G [41]
Gate drivers	Bootstrap supply voltage up to 118V	Texas Instruments LM5106 [42]
Microcontroller	Max PWM clock frequency 100 MHz	Texas Instruments TMS320F28377D [43]



(a) (b)

Fig. 8. Elements designed and built for the experimental setup. (a) Non-inverting buck-boost converter. (b) TMS320F28377D control card vertically mounted on the customized control interface.

IV. EXPERIMENTAL RESULTS AND DISCUSSION

A. Hardware Description

With the scope of comparing the benefit of the FLC technique vs. the linear cascaded control technique, a (continuous-conduction-mode) non-inverting buck-boost dc-MIC was designed and built (Fig. 8a). This converter is interfaced to a Texas Instruments TMS320F28377D digital microcontroller, via a custom designed control platform (Fig. 8b). The digital controller accurately measures the average inductor current, by timing the sampling to occur exactly at $\frac{T_{sw}}{2} \times d_1$, or $\frac{T_{sw}}{2} \times d_2$. Relevant data for the converter are reported in Table II.

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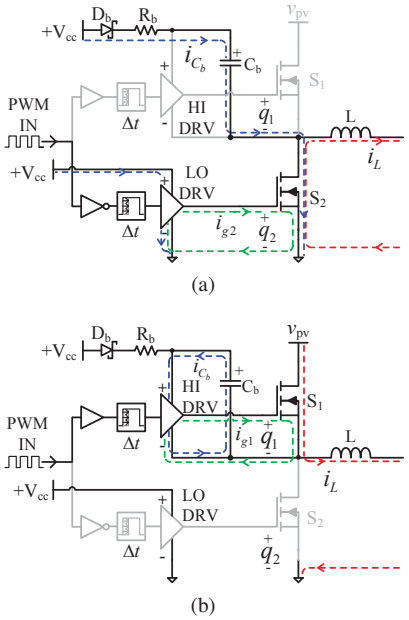

Fig. 9. dc-MIC gate driving circuit operation. (a) Lower switch S_2 is on (S_1 is off) and the bootstrap capacitor C_b is being charged by the auxiliary power source V_cc. (b) High side switch S_1 is on (S_2 is off), D_b is reverse biased, and the bootstrap capacitor C_b discharges to provide power to the high-side gate driver.

The dc-MIC prototype, in Fig. 8a, has its switching legs driven by Texas Instruments LM5106 [42] half bridge gate drivers, which turn on/off the high-side MOSFETs thanks to a bootstrap capacitor (C_b) powering the high-side gate driver. This solution was chosen because it is simple [44], economical and frequently encountered in practice for converters up to several kW [45], and in the PV application [46], [47]. Its major implication is due to the need for periodical recharge of the bootstrap capacitor, in the converter leg which is supposed to operate with the high-side MOSFET permanently turned on; according to Table I, this is the buck leg during boost operation of the converter, or the boost leg during the buck operation of the converter. In detail, when the converter (see Fig. 1 and Fig. 9) is in buck mode, then S_4 must be periodically turned off, by setting the driving signal q_4 to low. Similarly, when the converter is in boost mode, then S_1 must be periodically turned off, by forcing the driving signal q_1 to low. It was necessary to describe this operational detail, in order to understand the waveforms described in the second part of the results section, where q_1 and q_4 are also reported, and periodically set to low to allow the bootstrap capacitor recharge.

Finally, the converter is connected to a PV simulator (*Regatron TopCon* with *TC.LIN* post processing unit [48]) emulating the current vs. voltage *i-v* curve of a 100 W crystalline Silicon (cSi) PV module, according to the Standard EN 50530 [49]; the emulated PV module has a maximum power P_mpp = 100 W, at the MPP voltage V_mpp = 26 V and MPP current I_mpp = 3.84 A, while its open circuit voltage V_oc = 32.9 V and short circuit current current I_sc = 4.27 A. The dc-MIC load is implemented by an electronic dc load, Kikusui PLZ1004WH [50], operated in constant voltage mode.

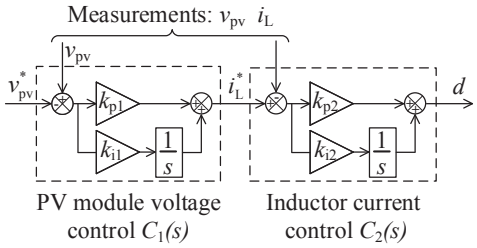

Fig. 10. Cascaded controller used for comparison purposes. The variable d at the controller output is either the buck duty cycle d_1 during buck operation (with $d_2 = 0$), or the boost duty cycle d_2 during boost operation (with $d_1 = 1$).

B. System Robustness Test

Section II-C highlighted the stability issues of the dc-MIC in buck mode, under the linear cascaded control scheme, and with the PV source in the CCR. To prove this concept and validate criteria (28), a linear cascaded controller was designed using the converter transfer functions presented in Section II-B. The linear cascaded controller is displayed in Fig. 10, where $C_1(s)$, with coefficients k_p1, k_i1, regulates the PV module voltage, while $C_2(s)$, having coefficients k_p2, k_i2, regulates the (average) inductor current. The proportional and integral gains were chosen to guarantee stability and ensure a performance trade-off between the converter response in the buck and in the boost mode, for different operating points of the PV module *i-v* curve. The coefficients are: k_p1 = 1, k_i1 = 1257 and k_p2 = 0.06, k_i2 = 792. Further discussion on the linear cascaded controller design is out of the scope of this paper, and can be referred to dedicated literature, such as [13]–[18], [38]. On the other hand, the FLC scheme parameters were chosen according to the framework proposed in Section III-C. The crossover frequency of the inner current loop was selected to be f_i = 10 kHz, and the crossover frequency of the outer PV voltage loop was chosen equal to f_v = 2 kHz. Using these values it followed that k_pi = 1.38 and k_ii = 87, for the (inner loop) current controller, while k_pv = 0.69 and k_iv = 9, for the (outer loop) voltage controller. The controller coefficients are quite different for the two compared control techniques. This difference is attributed to the design philosophy adopted. In fact, in the linear cascaded control case, the design is based on small-signal transfer functions. In contrast, in the feedback linearization case, the design is based on the linearization of the non-linear switching cycle averaged equations by means of non-linear control laws.

To verify the occurrence of instability under the linear cascaded control scheme, when the converter is operated in the buck mode, the proportional gain of the outer loop controller k_p1 was varied until it was far removed from its original design value, and was no longer complying with (28). The test was then repeated when the FLC scheme was applied. Also in this latter case, the proportional gain of the voltage controller k_pv was varied, showing no effect on the system stability. In this test, the dc-MIC was feeding a constant voltage electronic load, set to V_o = 15 V. The solar irradiation on the PV module emulator was set to 500 W/m^2; at such value of solar irradiation the PV module MPP voltage is V_mpp = 24.5 V.

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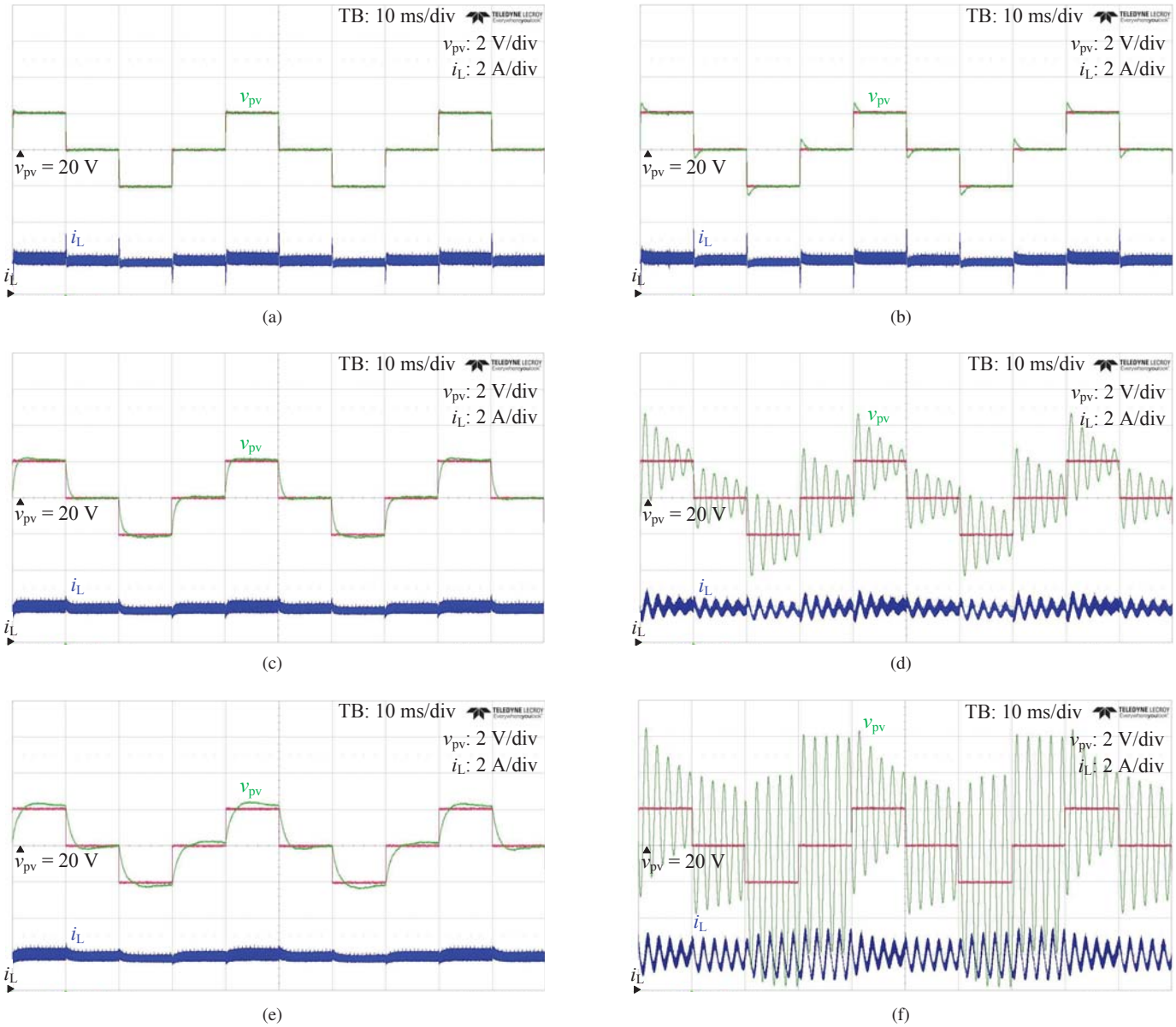

Fig. 11. PV module voltage regulation with the converter in buck mode, in the CCR, for varying proportional gain of the outer voltage loop controller and $V_o = 15$ V (left column: FLC controller, right column: linear cascaded controller). (a) $k_{pv} = 0.7$ (FLC). (b) $k_{p1} = 1$ (Linear Cascaded Control). (c) $25\% \times k_{pv} = 0.175$ (FLC). (d) $25\% \times k_{p1} = 0.25$ (Linear Cascaded Control). (e) $15.5\% \times k_{pv} = 0.1$ (FLC). (f) $17.5\% \times k_{p1} = 0.15$ (Linear Cascaded Control).

The dc-MIC input voltage reference was set to $v^*_{pv} = 20$ V, so that the dc-MIC operated with $V_{pv} < V_{mpp}$, i.e. in the CCR and in buck mode, since $V_{pv} > V_o$. Under these conditions for the linear cascaded control scheme, according to (28), stability is ensured if $k_{p1} > 0.13$.

Starting from a quiescent value of the input voltage $V_{pv} = 20$ V, a step of $\Delta v^*_{pv} = \pm 2$ V was given to the PV module voltage reference, v^*_{pv}, in order to test the converter response. Fig. 11a (FLC) and Fig. 11b (linear cascaded control) represent the step responses with the designed values of the controller gains. In Fig. 11c (FLC) and Fig. 11d (linear cascaded control), the proportional gain of the voltage controller was reduced to 25% of its original design value. With the FLC, applied in Fig. 11c, there is no substantial difference in the transient response, apart from a moderate increase in the settling time, compared to the case in Fig. 11a with full k_{pv}. When the dc-MIC input voltage is regulated by the linear cascaded control scheme, and the proportional gain of the voltage controller k_{p1} is only 25% of the initially calculated value, as in Fig. 11d, it is noticeable a large increase of the overshoot, settling time, and a decrease of the damping factor, indicating that the stability margin have been drastically reduced from the previous case with full k_{p1}, shown in Fig. 11b. Finally, when the proportional gain of the outer loop controller was reduced to about only 15% of its design value, the step response obtained with the linear cascaded controller, shown in Fig. 11f, clearly identifies the effect of a dramatically degraded stability margin, implying that the limit imposed by (28) is about to be violated. Fig. 11e shows the step response with a minimum value of k_{p1}, reduced to about 15% of its original design value,

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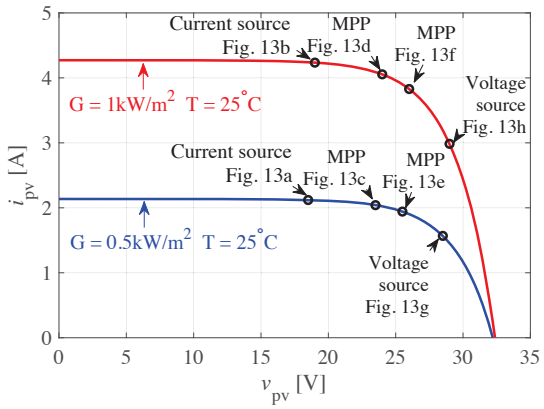

Fig. 12. Operating points on the PV module *i-v* curve at which different step responses have been observed.

with the converter regulated by the FLC scheme. Although the transient performance is slightly reduced compared to Fig. 11a (FLC and full k_{pv}) and Fig. 11c (FLC and 25% k_{pv}), it is apparent that the drastic decrease of the voltage controller proportional gain does not affect the system stability.

In summary, firstly, these tests proved the criteria found for the linear cascaded control scheme, according to which the system becomes unstable if the proportional gain of the voltage controller does not satisfy (28). Secondly, contrarily to cascaded control scheme, it was shown that when the dc-MIC is regulated by the FLC scheme, large variations of the voltage controller proportional gain do not hinder the stability, therefore the system is considerably more robust than with the linear cascaded control scheme.

C. Transient Performance Tests

The transient performance of the proposed FLC controller is now compared with the results given by the linear cascaded controller, designed around the small-signal converter transfer functions derived in Section II-B.

The converter response to input voltage reference steps is experimentally observed, when the FLC scheme or the linear cascaded control scheme is adopted. It is well-known that in the PV application, it is difficult for the converter to ensure a consistent dynamic performance, as this greatly depends on the quiescent point on the PV module *i-v* curve. For this reason the voltage regulation of the two compared control schemes is tested starting at different quiescent points on the PV module *i-v* curve. A reference step of $\Delta v_{\mathrm{pv}}^{*}$ = 2 V is given starting from a quiescent point in the CCR, around the MPP region, and in the CVR, as defined in Fig. 2a. The transient response have been recorded for both the buck and the boost operation. In the buck case, the solar irradiation on the PV simulator was set to G = 0.5 kW/m^2 (Fig. 12) and the dc-MIC output voltage was set to V_{o} = 15 V by means of a dc electronic load (Kikusui PLZ1004WH) operating in constant voltage mode. In the boost case, it was G = 1 kW/m^2 (Fig. 12) and V_{o} = 45 V. This choice of V_{o} was made in order to reflect a typical dc-MICs behavior, stepping up its output voltage when connected to a fully irradiated PV module and, conversely, stepping down its output voltage when connected to a shaded PV module, as illustrated in [5, Fig. 4c].

TABLE III
PV MODULE VOLTAGE STEP RESPONSE OVERSHOOT AND SETTLING TIME, WITH THE CONVERTER WORKING IN THE BUCK MODE (G = 0.5 kW/m^2, V_{o} = 15 V)

v_{pv}^{*} [V]	Overshoot [%]		Settling Time [ms]		Fig.
	Linear Cascaded	FLC	Linear Cascaded	FLC	
18.5 → 20.5	27.3	6	2	0.4	13a
23.5 → 25.5	23.7	11.8	2	0.4	13c
25.5 → 27.5	16.6	17	0.8	0.4	13e
28.5 → 30.5	5	12.8	2.5	0.8	13g
Standard deviation	9.8	4.5	0.7	0.2	

TABLE IV
PV MODULE VOLTAGE STEP RESPONSE OVERSHOOT AND SETTLING TIME, WITH THE CONVERTER WORKING IN THE BOOST MODE (G = 0.5 kW/m^2, V_{o} = 45 V)

v_{pv}^{*} [V]	Overshoot [%]		Settling Time [ms]		Fig.
	Linear Cascaded	FLC	Linear Cascaded	FLC	
19 → 21	27.3	0	1	0.4	13b
24 → 26	25.6	0	1	0.4	13d
26 → 28	28.3	0	1.4	0.6	13f
29 → 31	17.5	0	2.5	0.6	13h
Standard deviation	4.9	0	0.7	0.1	

The results reported in Fig. 13 display the response to step changes in the PV module voltage reference v_{pv}^{*}. Fig. 13a, Fig. 13c, Fig. 13e and Fig. 13g compare the results after the voltage reference is given a 2 V step, with the dc-MIC operating in buck mode. While in Fig. 13a the PV module quiescent point is in the CCR, in Fig. 13c and Fig. 13e it is around the MPP region, and in Fig. 13g it is in the CVR. The same can be said for Fig. 13b, Fig. 13d, Fig. 13f and Fig. 13h, respectively, when the dc-MIC is working in the boost mode. An important remark can be drawn from these results. In the case of linear cascaded control, where the controller has been designed around the small-signal transfer functions derived in Section II-B, the PV module voltage transient response is significantly different in each case, as it depends on the quiescent point on the PV module *i-v* curve. The difference in the performance is apparent, in terms of overshoot and settling time discrepancies. On the other hand, if the FLC scheme is adopted, the transient responses maintain a similar evolution in all cases, independently on the operating point on the *i-v* curve. Only in the case of Fig. 13e, the linear cascaded control scheme and FLC scheme produce similar results. With the FLC controller, the transient responses remain consistent when the converter is operating in buck mode. Also when the converter is operating in the boost mode, the transient responses present a consistent behavior, although their evolution is only slightly different from the one experienced in the buck mode.

Table III and IV report a summary of the overshoot and settling time parameters, related to the PV module voltage

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Fig. 13. PV voltage and inductor current behavior in response to PV voltage reference steps (green: FLC, blue: linear cascaded controller, pink: v_{pv}^*). (a) Buck mode in the current source region (18.5-20.5V). (b) Boost mode in the current source region (19-21 V). (c) Buck mode in the MPP region (23.5-25.5 V). (d) Boost mode in the MPP region (24-26 V). (e) Buck mode in the MPP region (25.7-27.5 V). (f) Boost mode in the MPP region (26-28 V). (g) Buck mode in the voltage source region (28.5-30.5 V). (h) Boost mode in the voltage source region (29-31 V).

transient responses displayed in Fig. 13. From observation of Table III-IV it is clear that, contrarily to the linear cascaded control, the FLC scheme ensures a transient performance independent of the quiescent point in the *i-v* curve.

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V. Conclusion

In this paper, the FLC technique was applied to design a non-linear controller for a non-inverting buck-boost PV module interfacing converter. Before outlining a framework for designing the FLC controller, the limitations of the traditional linear cascaded control scheme were discussed. The first limitation regarded the stability of the converter in the buck mode, which was shown to depend on the value of the voltage controller proportional gain. The second limitation is the undesired dependency of the transient response on the PV module quiescent point in the *i-v* characteristic.

In contrast, adopting the FLC technique, the converter operation was shown to remain stable regardless of any large variation in the voltage controller proportional gain, solving the problem of the buck mode instability when the PV module operates in the CCR. Moreover, with the FLC scheme, the PV module voltage regulation was demonstrated to occur with fast and consistent dynamics, independently of the quiescent point in the PV module *i-v* characteristic.

The performance improvement of the FLC scheme over the linear cascaded control scheme is attributed to the use of additional feedback signals. These signals allow execution of the derived non-linear control laws, canceling the system non-linearity and yielding similar transient performance regardless of the PV source and load operating points.

Compared to the linear cascaded control technique, which only needs the measurement of the PV module voltage and the average inductor current, the non-linear controller designed with the FLC technique requires additional measurement of the PV module current and the output voltage, in order to perform the control algorithm. This does not necessarily imply that additional sensors should be used, as the PV module current is often measured for MPPT purposes, while the converter output voltage can be monitored for protection purposes. The last observation regards the controller gains derived with the FLC technique, which have shown to depend on the value of the converter passive components. This demands a tight tolerance in the value of the passive components, or parameter estimation methods.

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